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A Ka-band calibratable phased-array front-end chip with high element-consistency

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Dear editor,

Active phased arrays are widely used in radar and communication systems due to their characteristics such as rapid wave beam steering, agile beamforming, and spatial power synthesis. The phased-array system contains a large number of elements. Three critical components in each element are precise amplitude control, precise phase control, and signal amplification.

Generally, amplitude control is implemented by attenuators that are usually formed by a large number of resistors, passive devices, switches, and other devices. However, the resistor is significantly influenced by process, voltage, and temperature (PVT) variation and it is difficult to calibrate each resistor. Passive devices usually occupy a large area and the switches introduce insertion loss [1]. Based on the above considerations, the attenuator is required to achieve high amplitude control accuracy with less PVT influence and area consumption. The phase shifter is usually utilized for phase control, which has similar considerations as the attenuator to achieve a high phase control accuracy.

The phased-array system that needs precise control requires accurate calibration capability and element consistency. The phase and amplitude mismatch between the elements reduces the main lobe gain and causes beam pointing deviation, thereby lowering the quality of the signal and the anti-jamming performance of the system. This study discusses the calibration technique of the attenuator and phase shifter with layout planning that is beneficial for the element consistency to implement a Ka-band 8-element phased-array transmit front-end chip.

System architecture. Figure 1(a) shows the layout planning of the proposed 8-element phased-array transmit front-end module. All-RF phased-array architecture (phase shifting in RF frequency) is adopted for better anti-interference performance. The module mainly consists of a 2-stage driver amplifier, a 1 to 8 power distribution network, and 8 phased-array elements. Each element includes a 5-bit attenuator, a reflection-type phase shifter (RTPS) [2], a 0/180° switching amplifier, a power amplifier, and other buffer stages. All amplifier modules adopt a differential structure with 50 Ω input and output ports, leading to individual design and simple cascade connection. A transformer-based broadband matching technology [3] is utilized in the amplifier stages to compromise the gain and bandwidth.

The measured attenuator of Element 1 when the phase shifter is set at the reference state shows that it achieves a 15.5 dB attenuation range with 0.5 dB step and the phase variation is less than 5.45° across 27.5–30.5 GHz. The measured phase shifter including the RTPS and 0/180° switching amplifier of Element 1 when the attenuator is set at the reference state shows a 360° phase-shifting coverage with the step of 5.625°.

Calibration of the attenuator and phase shifter. To reduce the area consumption, the PI/T network with a switch-embedded structure attenuator is adopted in this study. However, it is needed to solve two calibration problems: amplitude calibration and phase calibration. The deviation of the resistor in this structure introduces the amplitude error, especially for high attenuation states such as 4 and 8 dB attenuation, which may be larger than ±0.5 dB. While the amplitude error introduced by the low attenuation state is relatively small. In order to solve the deviation of the high attenuation states, a calibratable attenuation stage cascade strategy is proposed. In this study, the 4 and 8 dB attenuation states are divided into 3.5+0.5 dB and 7.5+0.5 dB, respectively. At the same time, an additional 1 dB calibration state is added to deal with insufficient attenuation. These amplitude calibration units including the 0.5 and 1 dB states can be bypassed or connected to the attenuation chain, thereby improving the attenuation accuracy.

For the phase calibration of the attenuator, as shown in Figure 1(b), three switched capacitors for compensation are introduced for the intermediate attenuation states (2 and 3.5 dB). When the switch of C_{scal} is turned on, the capacitor produces a positive phase shifting; when the switch of C_{pcal} is turned on, the capacitor produces a negative phase

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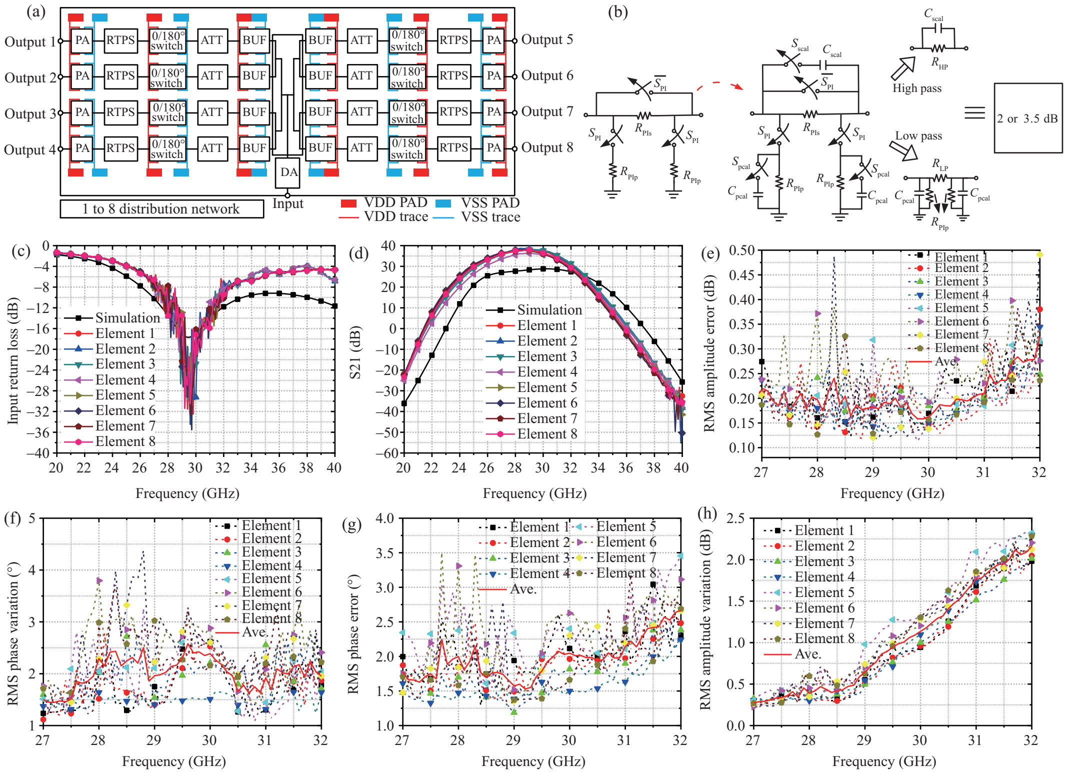

Figure 1 (Color online) (a) Layout planning of proposed 8-element phased-array transmit front-end module; (b) proposed PI-type unit with phase calibration capacitors; measured S11 (c) and S21 (d) for all elements at reference attenuation state; measured RMS amplitude error (e) and RMS phase variation (f) of Elements 1–8 when the phase shifter is set at the reference state; measured RMS phase error (g) and RMS amplitude variation (h) of Elements 1–8 when the attenuator is set at the reference state.

shifting. Changing the state of the compensation switched capacitors in the PI-type switch, the phase shifting introduced by the attenuator will be calibrated.

The cascaded RTPS and 0/180° switching amplifier are adopted to achieve accurate phase control. The 0/180° switching amplifier reduces the required phase shifting range of the RTPS, thereby improving the phase shifting accuracy. The phase shifting can be achieved by adjusting the PI-type capacitors in the RTPS. In this study, a 4-bit coarse switched-capacitor array and a 3-bit voltage controlled varactor are utilized to achieve 7-bit approximate continuous phase shifting, which is sufficient to achieve a 6-bit resolution even with the PVT deviation.

Layout planning. Figure 1(a) shows the layout planning of the proposed 8-element phased-array transmit front-end chip that is equally divided into two groups and arranged in mirror images. The input signal is averagely sent to 8 phased-array elements through the driver amplifier and 1 to 8 power distribution network. In order to improve element consistency, every two elements share a set of power and ground PADs, and their traces are arranged axisymmetrically in the core of the chip. With the above layout planning, good element consistency is achieved, as proved by the measurement.

Fabrication and measurement results. The Ka-band 8-element phased-array transmit front-end chip has been implemented in 65 nm CMOS (complementary metal-oxide-semiconductor). The chip size is 6.95 mm ×3.17 mm including the pads. The transmit front-end chip is measured via an on-chip probing system. The power supply is wired-bonded to the PCB (printed circuit board). DC voltages are provided by E3636A. The chip consumes a 1.66 A current from 1.2 V power supplies.

All 8 elements of the transmit front-end module can deliver higher than 12 dBm OP1dB power at 29 GHz. The average OP1dB of all elements is 12.4 dBm. As shown in Figure 1(c), the input return loss of all elements is better than 10 dB over 27.5–30.5 GHz, and all the elements show similar performance. Figure 1(d) shows that the front-end chip achieves about 36 dB gain for all the elements. Figures 1(e) and (f) show that all elements realize less than 0.49 dB RMS (root mean square) amplitude error and less than 4.27° RMS phase variation. The average RMS amplitude error and RMS phase variation of all elements are less than 0.24 dB and 2.5°, respectively. As shown in Figures 1(g) and (h), all elements realize <3.5° RMS phase error and <1.63 dB RMS amplitude variation over 27.5–30.5 GHz. The average RMS phase error and RMS amplitude variation of all elements are less than 2.25° and 1.41 dB, respectively. The measurements show that the proposed transmit front-end chip achieves competitive performance compared with the state-of-the-art and shows good element consistency.

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