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A 24.25–27.5 GHz 128-element dual-polarized 5G integrated phased array with 5.6%-EVM 400-MHz 64-QAM and 50-dBm EIRP

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With the rapid evolution of mobile communication technology, the data volume of new mobile services is growing exponentially, resulting in an explosive demand for increased data throughput [1,2]. The 5G millimeter-wave (mm-Wave) frequency bands offer massive spectrum resources, which can greatly improve the communication rate and provide numerous possibilities for ultra-high-speed communication services [3–6]. Compared to the traditional GaAs- or GaN-based implementation, the mm-Wave phased array based on the silicon complementary metal oxide semiconductor (CMOS) technology enables large-scale network coverage for mm-Wave 5G base stations at a low cost. The mm-Wave 5G uses 24.25–27.5 GHz as the operation band, covering the 3GPP 5G NR FR2 N258 band. Owing to the trade-off between the size of the mm-Wave array and the number of beamformer ICs, ensuring a low thermal density chip distribution along with an optimal performance of the phased-array antenna can be challenging. An enhanced communication data rate can be achieved by using a dual-polarized antenna, which offers the advantage of reducing the number of the two independent antenna units [7]. However, it is difficult to implement an integrated dual-polarized antenna for an overall small physical size. To compensate for the influence of the increased path loss at the mm-Wave, the linear output power of the phased-array antenna must be guaranteed. Furthermore, the cross-polarization performance and the large angle scan degradation of the dual-polarized antenna are also challenging.

In this study, we propose a 24.25–27.5 GHz 128-element time division duplexing dual-polarized (+45° pol/−45° pol) phased-array antenna for mm-Wave 5G communications. It is based on the silicon-based 65-nm CMOS 4-channel (two horizontal-polarization and two vertical-polarization, 2H2V) beamformer integrated circuit (IC). The power supply circuit, logic control circuit, radio frequency (RF) feed circuit, and stacked patch antenna are fabricated on a high-frequency multi-layer printed circuit board (PCB). Each transceiver (TRX) channel of the beamformer IC uses a T-type junction feed to two antenna units, thereby reducing the number of the chips by half and realizing low thermal density distribution for the robustness of the proposed 128-element dual-polarized array. By adopting the low-loss chip packaging technology and integrated antenna methodologies, this study achieves the effective isotropic radiated power (EIRP) of over 49.7 dBm of the dual-polarized antenna while meeting the specification of the 3GPP standard (error vector magnitude (EVM) < 5.6%, 64-QAM) with 400-MHz modulation.

5G phased-array IC design and characterizations. The antenna consists of thirty-two 4-channel (2H2V) dual-polarized beamformer ICs. The CMOS dual-polarized beamformer IC consists of two horizontal-polarized channels and two vertical-polarized channels with an operating bandwidth from 24.25 to 29.5 GHz [8]. The architecture diagram and chip micrograph are shown in Figure 1(a). The fan-out wafer level packaging (FOWLP) process is employed to reduce the packaging loss at the mm-Wave band. The packaged chip size is 6.7 mm × 5.25 mm. Each chip channel has an independent transceiver amplifier chain and amplitude/phase control circuits. The beamformer IC is implemented using the RF phase-shifting architecture for low power consumption. The beamformer IC phase and the gain adjusting range are 360° and 31.5 dB, respectively, with a 6-bit resolution (5.625°/0.5 dB, respectively). A standard serial peripheral interface (SPI) with 256 pre-stored beams is implemented for fast beam switching. A single-polarized CMOS 4-channel chip of the same architecture is applied as the driver stage of the phased array. Its 4-transceiver chains can be directly connected to the quarter unit of the +45° or −45° polarization chain, thus reducing the multi-layer board area occupied by quartering the power divider. In this study, the DC supply voltages of the dual-polarized

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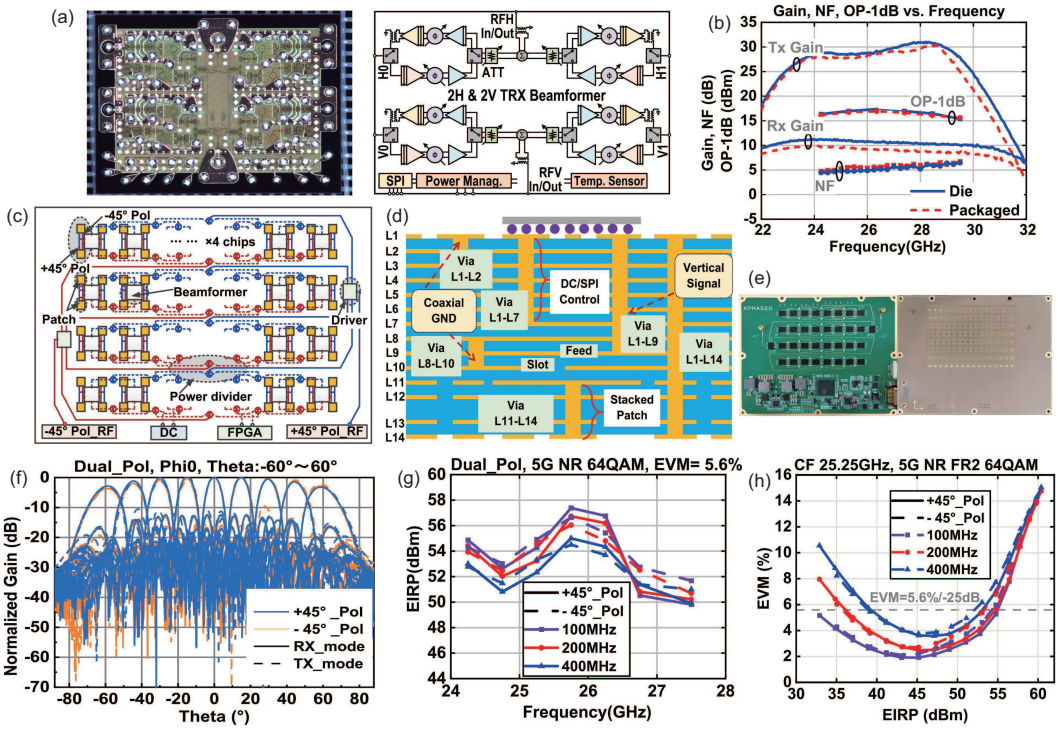

Figure 1 (Color online) (a) The architecture and micrograph of the dual-polarized beamformer IC; (b) the beamformer IC measurement results; (c) the architecture of the phased-array antenna; (d) the cross section of the antenna PCB; (e) the top and bottom views of the antenna; (f) the measured normalized radiation pattern of the antenna (phi = 0°, theta = −60° to +60°); (g) measured EIRP versus frequency with 5G NR modulation; (h) EVM (64-QAM) versus output power at 25.25 GHz.

beamformer ICs are 1.0 and 1.8 V. The DC-DC converter chip converts the 12 V power supply from the external input into the operating voltages of the chips on the antenna board. The typical measurements of the beamformer IC are shown in Figure 1(b). The frequency responses of the S-parameter agree well with those of the unpackaged chip. At 25.75 GHz, it presents a measured output 1-dB compression point of 16.8 dBm with a gain of 27.9 dB in the TX mode. In the RX mode, the single-path gain is 9.2 dB with a noise of 5.5 dB. By adopting the FOWLP technology, the output power loss is below 0.5 dB as compared to the on-wafer measurement results, implying reduced packaging loss.

Dual-polarized phased-array antenna implementations. Dual-polarized antenna is the critical building block of the mm-Wave 5G base station. The RF interface of the antenna is connected to the external up/down frequency conversion module to realize the complete active antenna unit function of the base station. As shown in Figure 1(c), the mm-Wave dual-polarized antenna consists of a multi-layer PCB, a dual-polarized feed network, CMOS beamformer ICs, driver chips, a power supply system, and a logic control circuit. The 128-element dual-polarized antenna PCB is built on a low-cost high-frequency substrate material (Dk = 3.62, Df = 0.005 @29 GHz) with a physical size of 155 mm × 120 mm. By adopting the high-performance CMOS beamformer IC and utilizing the high-frequency multi-layer PCB, the area of the RF channel is reduced, and the small size of the antenna array is achieved. Both the +45° polarized and the −45° polarized array employ 128 antenna elements distributed on the X and Y axes, with a grid spacing of 5.5 mm (0.50λ @27.5 GHz) and 8.0 mm (0.73λ @27.5 GHz), respectively. The dual-polarized array has a maximum azimuth/elevation of ±60°/±15°, which meets the requirement of the base station installation. The cross section of the antenna PCB is shown in Figure 1(d). The dual-polarized 1:8 Wilkinson power divider, beamformer ICs, circuit devices, connectors, and other components are located on L1. Thin film resistors are used as the Wilkinson power divider isolation resistors, while the feed network is implemented with a microstrip line. The 4-channel (2H2V) beamformer ICs are welded onto the L1 layer. L2 is used as the RF ground of grounded coplanar waveguide (GCPW). L3–L7 are mainly used to distribute digital SPI control lines and DC power supply. The complete L4 is employed as the ground plane to avoid low-frequency crosstalk. L8 is used for the antenna ground plane. L9 is the feed circuit of the antenna, which is connected to the TRX port of the chip through the vertical coaxial and excites the patch antenna through the slot of the L10 layer. The antenna is implemented as a dual-polarized stacked patch antenna on L11–L14. With an additional equivalent capacitance, the antenna demonstrates the enhanced bandwidth with the simulated voltage standing wave ratio (VSWR) of below 1.5 across 24.25–27.5 GHz. The simulated radiation efficiency of the phased-array antenna is above 85%. The TRX port of the CMOS chip is fed to the two antenna units using a T-type junction, which can increase the gain of each polarization by 3 dB. The realized gain of the 128-element array is over 25.5 dB. The advantage of this design is the reduction of the required beamformer ICs for the antenna while satisfying the beam scanning range of the array. Consequently, the thermal density and power consumption are both reduced. The top and bottom views of the dual-polarized phased array are shown in Figure 1(e).

Measurement results. The beamformer ICs are welded to the multi-layer PCB array after being tested. The dual-polarized 128-element phased-array antenna was calibrated

and measured in the far-field scenario. At 25.75 GHz, the original amplitude distribution of the dual-polarized antenna shows variations below ±2.7 dB and ±2.5 dB across all channels with the TX and RX modes, respectively. Moreover, there is no performance failure among all channels. This is attributed to the final test of the packaged chip via automatic test equipment with a socket before the surface mounted technology welding process. After the channel phase calibration, the phase variation of the array is less than ±9.5°. The radiation pattern of the antenna at the maximum gain is measured in the TX and RX modes. Under the +45°/−45° polarized mode, the normalized gain at 25.25 GHz across the azimuth angles of −60° to +60° is depicted in Figure 1(f). The azimuth pattern demonstrates a 3-dB beamwidth of 6.5°, and the performance at a large scanning angle (+60°/−60°) is degraded by 4.0 dB. The EIRP of the dual-polarized array with the 400-MHz bandwidth 64-QAM modulation is shown in Figure 1(g). Across the full operating band, the output power is higher than 49.7 dBm. Figure 1(h) presents the measured 64-QAM EVM versus output power at 25.25 GHz. The array covers the modulation bandwidths of 100-MHz/200-MHz/400-MHz (5G NR 64-QAM, EVM < 5.6%) with the EIRP between 52.5 and 55 dBm. The dual-polarized array introduces the parasitic patch to minimize cross-polarization. The antenna shows over 20 dB of cross-polarization rejection at 25.75 GHz across the angles of ±60°/±15° in the azimuth/elevation plane.

Conclusion. In this study, we present a dual-polarized phased-array antenna based on 65-nm CMOS beamformer ICs that realizes a low thermal density distribution of 128 units (i.e., 64 RF channels). The output power of the antenna is higher than 49.7 dBm across 24.25–27.5 GHz with the 5G NR 400-MHz 64-QAM modulation (EVM < 5.6%). When the antenna is scanned at a large angle (+60°/−60°) in the azimuth pattern, the gain is degraded by 4.0 dB.

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Supporting information Videos and other supplemental documents. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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