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Van der Waals heterostructure tunnel FET with potential modulation beyond junction region

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Dear editor,

• LETTER •

State-of-the-art semiconductor technology is approaching the atomic scale, greatly boosting the switching behavior of transistors towards the physical limit of the thermionic emission mechanism [1, 2]. A fundamental revolution is needed to break this limit and reduce power dissipation. Owing to the band-to-band tunneling mechanism, this goal can be achieved by tunnel FET (TFET), in which carriers are injected into the channel in a "cold" manner rather than through thermal injection [3]. TFETs usually suffer from weak tunneling problems, which relate directly to the degree of energy band bending and require a steep doping gradient and robust gate control ability near the tunneling interface [4].

Successful mechanical exfoliation technology has realized many novel two-dimensional (2D) materials and structures that exhibit fascinating physical and electrical properties [5]. Among them, vertically stacked 2D materials forming van der Waals heterostructures (vdWHs) have strain-free, clean, and sharp heterointerfaces, making them suitable for tunnel devices. The first demonstration of the gate-tuned tunneling was the p-Germanium/MoS₂ vdWH TFET, in which the gate covers the entire channel region, and a sharp current increase is observed with increasing gate voltage (V_g) [6]. On the other hand, vdWHs with gapped band structures at both sides are usually used to build vertical p-n junctions later because of the low gate participation in the FET behaviors.

Inspired by this phenomenon, this study designed a vdWH TFET with gate modulation beyond the junction region. The TFET requires a vdWH with the type-III band alignment to keep the tunneling window normally open. At the same time, the off/on state is achieved by potential modulation of the single material regions. Using the WTe₂/HfS₂ TFET as an example, the channel consists of the monolayer WTe₂ and HfS₂ and their van der Waals (vdW) junction region which are the type-III band alignment. The first-

principles density functional theory (DFT) was adopted to assess the electronic properties of the 2D materials and the maximally localized Wannier function (MLWF) method was used to construct the tightbinding (TB) Hamiltonian of the unit cell from the DFT wavefunctions. The precision problem caused by the poorly localized Wannier orbitals was overcome by enlarging the supercell of the vdWH to break the nearest-neighbor limitation and incorporate more bondto-bond interactions. The enlargement size was tunable according to the band structure comparison between the Wannier restoration and the original DFT result. The Hamiltonian model of the hetero channel from the DFT-MLWF method was constructed by first obtaining the periodical Hamiltonian matrices of the heterostructure cell and then artificially extracting the matrices of the monolayer WTe_2 and HfS₂ from the heterostructure's, maintaining the matrix size. The simulation results verified the difficulty of tuning the interlayer potential difference at the junction regions and the validity of the proposed channel potential modulation strategy by exhibiting excellent switching behavior in the WTe_2/HfS_2 vdWH TFET.

Figure 1(a) shows the device model. The bottom and top layers of the channel consisted of the WTe_2 and HfS_2 , covered by two gates with opposite supply voltages and separated by the 1 nm oxide layers. The device channel can be divided into three regions: the monolayer WTe₂, WTe₂/HfS₂ vdWH, and monolayer HfS₂. The DFT density of states (DOS) of the three-channel regions were calculated independently, as shown in Figure 1(b), in which the Fermi levels were moved to zero, and the energy interval and Gaussian broadening factor were all 1 meV. The non-zero DOS near the Fermi level of the junction region indicates a carrier accumulation phenomenon and induces the carrier density differences at the mono/double-layer interfaces. The deformation charge densities in Figure 1(c) verify the interlayer charge transfer within the junction region, leading to hole and electron accumulation at the WTe_2 and HfS_2 layers. Therefore, the initial built-in potential and carrier distribu-

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Figure 1 (Color online) (a) Device model of the WTe₂/HfS₂ vdWH TFET. (b) DOS of the single layer WTe₂ and HfS₂ and their vdWH from the DFT. The x scale for each material was $0-4 \times 10^3 \text{ eV}^{-1}$. (c) Deformation charge densities at the vertical direction when the interlayer charge transfer was considered. (d), (e) Free carrier and band structure of the TFET channel with zero source, drain, and gate voltages and calculated from (1)–(3). The red and blue solid lines in (e) show the calculated bands and the dashed ones correspond to the abrupt and graded band limits. (f)–(j) Transfer characteristics and transport details of the WTe₂/HfS₂ vdWH TFET at $V_d = 0.3$ V with different lateral junction limits: (g), (h) abrupt junction; (i), (j) graded junction. At (g)–(j), the WTe₂ and HfS₂ bands are denoted by the red and blue lines. The energy-resolved current spectra and DOS participating in the transport are shown as the black lines and the background yellow colors.

tion of the device should be treated carefully by resolving self-consistently the one-dimensional Poisson and free carrier density equations:

$$dV(x)/dx = q[n(x) - p(x)]/\varepsilon_0\varepsilon_r,$$
(1)

$$n(x) = \int_{E>E_f}^{+\infty} \text{DOS}(E) / \left[1 + \exp\left(\frac{E - E_f - V(x)}{k_0 T}\right) \right],$$

$$p(x) = \int_{-\infty}^{E < E_f} \text{DOS}(E) / \left[1 + \exp\left(-\frac{E - E_f - V(x)}{k_0 T}\right) \right],$$
(3)

where V is the potential of the material layers within the channel, $\varepsilon_r = 3.3$ and 4.3 for the WTe₂ and HfS₂, respectively, and T is the room temperature. All external voltages were zero and the potentials at the junction regions were obtained from the DFT results, remaining unchanged during the calculation. From the carrier density results in Figure 1(d), the junction region possesses many carriers compared to the monolayers and the lateral transfer was observed. Note that the transferred carriers are not strictly "free" because a built-in electric field will be generated at the vdW gap [7], which is neglected in the carrier distribution calculations. The electric field can hinder the carriers' lateral movement and induce strong interlayer coupling which may screen external vertical electric fields. Figure 1(e) presents the initial band structures of the TFET before the quantum transport simulation which were generated by the superposition of the potentials and intrinsic bands. The following simulation solved the built-in electric field neglection

by considering the abrupt and graded lateral junction limits ① and ②. Note that the band inversion already existed at the junction region (the valence band edge of WTe₂ energetically exceeded the conduction band edge of HfS₂) because of the type-III band alignment. In other words, the tunneling window maintained a normal opening in this region.

Figure 1(f) presents the transfer characteristics of the WTe₂/HfS₂ vdWH TFET considering the abrupt and graded initial junction potential shapes at $V_d = 0.3$ V. For the abrupt junction, the drain current (I_d) first decreased to $4.1 \times 10^{-12} \ \mu A \cdot \mu m^{-1}$ at $V_g = 0.55$ V. Subsequently, it increased rapidly to $1.7 \ \mu A \cdot \mu m^{-1}$ within only 0.1 V V_g range, exhibiting an extremely low subthreshold swing (SS) of $3.8 \ mV \cdot dec^{-1}$. After a sudden increase, the current was kept at a high level and exceeded $4.8 \times 10^2 \ \mu A \cdot \mu m^{-1}$. Moreover, the off- and on-state currents of the TFET with the graded junction were 3×10^{-12} and $1.5 \times 10^3 \ \mu A \cdot \mu m^{-1}$, reaching an on-to-off ratio of 5×10^{14} , even better than that with the abrupt junction.

Figures 1(g)-(j) show the transfer behaviors of the TFETs, in which the two subplots (left and right) correspond to the abrupt and graded initial junction potential cases. The subplots were generated by the superposition of three kinds of information: the band structures under the supply voltages shown in red and blue lines; the energy-resolved current spectra are shown in black lines; the DOS participating in the transport is shown as the background yellow colors. Clearly, the transport in Figure 1(g) is induced mainly by the valence-to-valence and conduction-to-conduction band tunneling through the gap states of the

junction, which may be caused by the material edges. The current is then eliminated by increasing V_g before 0.55 V because of the staggered band alignment shutting down the tunneling. Note that the band inversion at the junction region does not contribute to transport at this V_g range because of the energy mismatch. With a continued staggering, the valence band of the monolayer WTe₂ reached the conduction band of the monolayer HfS₂ energetically. The band-to-band tunneling (BTBT) tunneling path was opened, resulting in a considerable increase in current, as shown in Figure 1(h). In comparison, the leakage current at small V_g can be restrained by the graded initial potential shape. The tunneling current at $V_g = 0.8$ V was also larger because of the up and down shifted bands of the monolayer regions.

As a response to V_g , the bands of monolayer WTe₂ and HfS₂ were moved up and down by 0.6 and 0.7 eV, respectively, at the abrupt junction case. However, the values were only 0.1 eV at the junction region, confirming the much weaker potential modulation ability of the gates at this region. The inefficient junction potential tuning can be attributed to the excessive charges that screen the electric field. On the other hand, high voltages are still needed to switch the band alignments of vdWHs regardless of the screening effect, considering the stable vdW gaps between the layers (3–8 Å) [5].

The interlayer potential differences are difficult to induce at vdWHs owing to the screening effect and small vdW gaps. Therefore, instead of the difficult band alignment modulation at the junction regions, a new switching strategy for the vdWH TFETs was proposed because the on- and offstates are controlled by the potentials of the single material regions. Utilizing the DFT-MLWF-quantum transport simulation flow, excellent switching behavior was observed in the WTe₂/HfS₂ vdWH TFET. From mechanism analysis, the TFETs suitable for this switching strategy only require the following: (1) vdWHs with the type-III band alignment and (2) sufficient single material regions for the potential modulation. The strategy offers a new opportunity for the low power consumption logical application of the vdWHs.

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