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# Efficient polar coding scheme and implementation with shared information bits

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Dear editor,

Polar codes invented by Arıkan [1] can achieve the capacity of symmetric binary-input discrete memoryless channels (B-DMCs) with an infinite code length. However, it suffers from unsatisfactory performance with a finite code length [2]. The performance degradation of polar codes with a finite code length is caused by the inadequate polarization phenomenon; therefore extensive polar coding schemes are proposed to protect the semi-polarization channels in recent years. An inter-frame polar coding scheme was proposed in [3]. It utilizes dynamic frozen bits to protect the weak polarization channels but suffers from unsatisfactory complexity. A partially information coupled (PIC) scheme was proposed in [4] as an alternative polar coding scheme to protect the semi-polarization channels with coupled information bits, but its performance and complexity can be further improved.

In this study, an efficient polar coding scheme is proposed to improve the performance of polar codes with a finite code length, which is called polar codes with memory (PCM) scheme. The PCM scheme deploys some shared information bits (SIBs) in the same position of two underlying blocks. When one block is decoded incorrectly and the other is decoded successfully, the succeeded block offers the failed block hard estimations of the SIBs. Then a new-round decoding is performed to recover the failed block. Furthermore, a generalized version of PCM (G-PCM) scheme is proposed to save code rate loss for the PCM scheme with multiple underlying blocks. The PCM scheme can employ any conventional decoder of polar codes, such as the successive cancellation (SC) decoder [1], belief propagation (BP) decoder [5], or cyclic redundant check (CRC) aided successive cancellation list (CA-SCL) decoder [6]. For ease of description, we use PCM-SC-$m$ to refer to the proposed PCM scheme with the SC decoder and $m$ underlying blocks. Similarly, PCM-BP-$m$ and PCM-SCL-$m$ refer to the PCM scheme with $m$ blocks based on the BP and CA-SCL decoder, respectively. Numerical results show that with the code length $N = 1024$ and code rate $R = 0.5$, the PCM-SCL-2 scheme with list size of $L$ achieves a comparable performance with the conventional CA-SCL decoder with list size of $2L$. Hardware implementation results also show that the PCM with the fast simplified SC (PCM-FastSSC) decoder achieves 4.3× more area efficiency compared with the fast simplified SC flip (Fast-SSCF) decoder [7].

*Efficient PCM scheme.* Let $v_1^N$ denote a vector $(v_1, v_2, \ldots, v_N)$, and let $N = 2^n (n \geqslant 1)$ denote the code length of polar codes. Let $u_1^N$ represent the source vector consisting of $K$ information bits and $N - K$ frozen bits. Then the code rate of polar codes is $R = K/N$. Let set $\mathcal{A}$ present the indices of the information bit channels, and then $u_{\mathcal{A}}$ is a subvector of the vector $u_1^N$ that takes elements of it from the set $\mathcal{A}$. The basic details of polar codes can be found in Appendix A. Figure 1(a) shows the system model of PCM scheme with the SC decoder. For clarity, we define $K_{\rm crc}$ as the number of CRC bits. Let $K_{\rm p}$ denote the number of the SIBs, and then there are $K_{\rm i} + K_{\rm p}$ information bits in each underlying block.

In the encoding process, the input source bits are first divided into chunks with $2K_{\rm i} + K_{\rm p}$ source bits. Then each chunk is divided into two source bit blocks: Block Odd (with $K_{\rm i} + K_{\rm p}$ source bits) and Block Even (with $K_{\rm i}$ source bits). Block Even takes $K_{\rm p}$ SIBs from Block Odd to constitute a complete source bit block with $K_{\rm i} + K_{\rm p}$ source bits. In this way, there are clearly the same $K_{\rm p}$ SIBs which are both included in Block Odd and Block Even. These SIBs will constitute the subvector $u_{\mathcal{B}}$ in the encoding process of polar codes, where $\mathcal{B}$ is a subset of the information bit set $\mathcal{A}$. Finally, Block Odd and Block Even pass the CRC encoder module and the polar encoder module, yielding a pair of codewords to be transmitted through the channel. The

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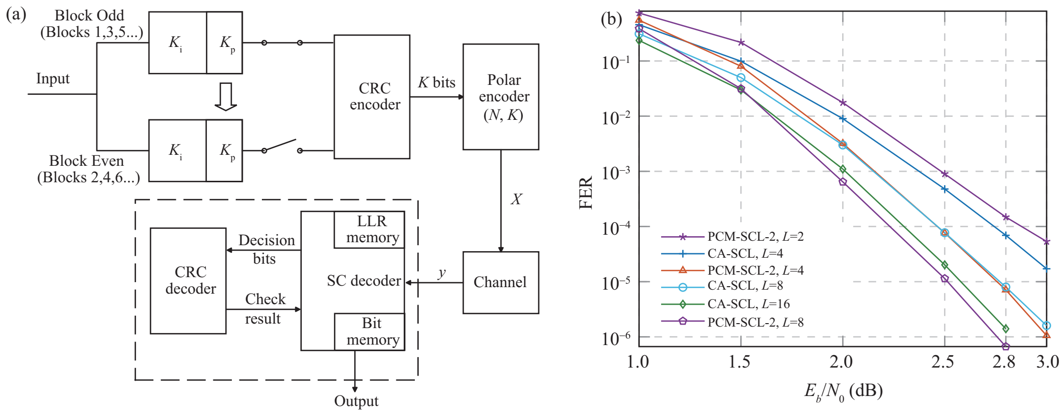


**Figure 1** (Color online) (a) System model of the PCM scheme with SC decoder and (b) FER performance of the PCM-SCL-2 scheme with $N = 1024$ and $R = 0.5$.

decoding strategy is provided in Appendix B.1.

The performance of the PCM scheme is directly affected by where to position the SIBs and how many SIBs are selected. The principles for choosing appropriate SIBs for PCM scheme are provided in Appendix B.2. Let $P_B$ denote the error probability of the underlying block with information set $\mathcal{A}$, and $P_b$ represent the error probability of the underlying block with the information set $\mathcal{A}' = \mathcal{A} \setminus \mathcal{B}$, and the error probability of the PCM scheme is expressed as

$$P_{\text{new}} = P_B^2 + (1 - P_B)P_b. \tag{1}$$

The error performance analysis can be found in Appendix B.3. The complexity analysis of the PCM scheme is offered in Appendix B.4.

*PCM scheme with multiple underlying blocks.* The PCM scheme with two underlying blocks can be directly extended to the D-PCM scheme with multiple underlying blocks ($m > 2$), with each block containing the same $K_{\text{p}}$ SIBs. The D-PCM scheme can be found in Appendix C.1. The main drawback of the D-PCM scheme is its heavy code rate loss. In order to reduce the code rate loss, the G-PCM scheme is proposed, in which the SIBs of each underlying block can be recovered by modulo 2 addition with the SIBs of the other $m-1$ underlying blocks. The G-PCM scheme can be found in Appendix C.2.

*Numerical results.* Figure 1(b) shows the frame error rate (FER) performance of the PCM-SCL-2 scheme with $N = 1024$, $K = 548$, $K_{\text{p}} = 40$. The code rate is $R = 0.5$. Additive white Gaussian noise (AWGN) channel and binary phase-shift keying (BPSK) modulation are utilized. The bit channel reliability sequence is generated with Tal-Vardy construction [8] at a designed signal-to-noise ratio of 2 dB. A polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$ in the 5G standard is used for the CRC modules. From Figure 1(b), we can draw several observations. First, the PCM-SCL-2 scheme with list size of 2 achieves a close performance (less than 0.15 dB) as the conventional CA-SCL decoder with list size of 4. Second, the PCM-SCL-2 with list size of 4 achieves a consistent performance with the conventional CA-SCL decoder with list size of 8. Finally, the PCM-SCL-2 scheme with list size of 8 outperforms the conventional CA-SCL decoder with list size of 16. More numerical results are in Appendix D.

*Hardware implementation.* Hardware implementation is presented in Appendix E.

*Conclusion.* In this study, a PCM scheme employing conventional decoders of polar codes is proposed. By sharing a certain amount of information bits between a pair of blocks, this scheme can significantly improve the FER performance of the conventional decoders for polar codes with finite code length. Results show that for the block length of $N = 1024$, the PCM-SCL-2 scheme with list size of $L$ can match the FER of the CA-SCL decoder with list size of $2L$.

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**Supporting information** Appendixes A–E. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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