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Improved transport properties and mechanism in recessed-gate InAlN/GaN HEMTs using a self-limited surface restoration method

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Abstract The etching process of high-performance recessed-gate InAlN/GaN high-electron mobility transistors (HEMTs) has been actively researched. This paper proposes a post-etching self-limited surface restoration method that effectively suppresses the etching damage, enhancing the transport properties of recessed-gate InAlN/GaN HEMTs. We fabricated planar-gate devices, inductively coupled plasma (ICP)-etched devices, and post-etching-treated (PET) devices. The damage caused by the ICP etching process severely deteriorated the transport properties of the devices. However, the post-etching process effectively inhibited the etching damage and improved the device transport properties. Through temperature-dependent tests and a simulation, the change in the peak transconductance was compared among different devices. The temperature-dependent optical phonon scattering and impurity-dependent remote charge scattering mechanisms were analyzed. The results confirmed that the etching damage significantly affected the channel electron scattering mechanism. The field-effect mobility showed a linear relationship with temperature, and the optical phonon scattering model illustrated that the field-effect mobility decreased with increasing temperature. The etching damage caused a decrease in the field-effect mobility from 1075.5 to 699.1 $cm^2/V{\cdot}s$, which increased the fitting error between this empirical line and the optical phonon scattering fitting curve from 0.086 to 0.948, similar to the remote charge scattering fitting curve. The combined error range is from 0.896 to 0.054.

Keywords GaN, InAlN/GaN HEMTs, etching damage, scattering mechanism

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1 Introduction

GaN-based high-electron mobility transistors (HEMTs) have the advantages of high-power density, high efficiency, and compact size. Thus, they are promising candidates for high-speed and high-power electronic devices [1–3]. To enhance the gate control on a conductive channel and the gain of a radio frequency device, the thickness of the barrier layer should be reduced, thus reducing the gate-channel distance [4]. Because of the considerable spontaneous polarization effect, the InAlN/GaN heterostructure can supply a higher two-dimensional electron gas (2DEG) density with a thinner barrier than the conventional AlGaN/GaN heterostructure. The spontaneous polarization difference and the conduction band discontinuity between the InAlN barrier layer and the GaN substrate are significantly larger than those of the conventional AlGaN/GaN heterojunction. The theoretical calculation results predict that the 2DEG area density of the InAlN/GaN heterojunction is as high as 2.7×10^{13} cm^{-2}, which is significantly higher than the areal density of 1.0×10^{13} cm^{-2} in the AlGaN/GaN heterojunction. Because of the higher carrier density, the carrier mobility in the InAlN/GaN heterojunction is lower than that in the AlGaN/GaN

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heterojunction. Compared to traditional AlGaN/GaN HEMTs, InAlN/GaN HEMTs usually operate in the depletion mode with higher pinch-off voltage owing to the greater polarization effect [5,6]. In practical applications, if it is used as a switching device, the channel should be maintained in a normally-off state to meet the system safety requirements. Therefore, recessed-gate InAlN/GaN HEMTs have excellent development prospects in E-mode devices. Therefore, research on the etching process of high-performance recessed-gate InAlN/GaN HEMTs has been actively conducted.

The gate recess in GaN-based technology is commonly achieved by using Cl_2 or Cl_2/BCl_3 plasma etching. However, dry etching causes surface damage at the interface of the barrier because of the bombardment of high-energy ions and the presence of reactive substances. This surface damage affects the device electrical characteristics and reliability, such as a sharp drop in the electron mobility, a decrease in the trans-conductance, or an increase in the gate leakage current [7–10]. To suppress the influence of etching damage on device characteristics, several low-damage etching methods and post-etching treatment methods were researched for the interface of the barrier, such as atomic layer etching and oxygen plasma or fluoride-based plasma treatment and wet treatment [11–16]. The atomic morphology of the InAlN material surface is not particularly desirable [17] because its etching damage is easy to cause. This paper proposes a method of repairing the etched interface using a self-limited surface restoration method, which is used to suppress the etching damage of the InAlN interface.

In this study, planar-gate devices, conventional inductively coupled plasma (ICP) etching process recessed-gate devices, and ICP etching process with post-etching treatment (PET) recessed-gate devices were fabricated. The transmission characteristics of multiple InAlN/GaN HEMT samples were extracted and analyzed, and the influence of ICP etching damage on the electronic transmission characteristics of the devices was studied. The electronic transmission characteristics of the devices can be affected by various mechanisms. Thus, to study the effects related to the etching process in comparison with ordinary devices, we used conventional ICP etching to process the devices under specific conditions and provided a PET control group. The trans-conductance of these three types of devices was obtained and compared. The results of the analysis showed that the abnormality of carrier transport characteristics is caused by the decrease in the device mobility. After conducting electrical tests at different temperatures, through a simulation and fitting analysis of the conditions affecting the mobility, the transition of the scattering mechanism caused by etching damage was obtained.

2 Device fabrication

InAlN/GaN epitaxial layers used in this work were grown on 3-in SiC substrates by molecular beam epitaxy, consisting of an 80-nm-thick AlN nuclear layer, 2-μm-thick GaN unintentionally doped (UID) buffer layer, 1-nm-thick AlN interlayer, and 2-nm-thick GaN cap layer on a 12-nm-thick $In_{0.17}Al_{0.83}N$ barrier layer. The Hall measurement room temperature shows a sheet carrier density of 1.98×10^{13} cm^{-2}, mobility of 1468 $cm^2/V \cdot s$, and sheet resistance of 228 Ω/sq. The source and drain ohmic contacts were fabricated with e-beam evaporation of Ti/Al/Ni/Au, lift-off process, and rapid thermal annealing at 820°C in N_2 for 50 s twice. An ohmic contact resistance of approximately 0.6 Ω·mm was derived using the transmission line passivation with plasma-enhanced chemical vapor deposition (PECVD). The gate foot area was defined by removing the SiN layer with ICP etching in CF_4 plasma. CF_4/O_2 mixed plasma was used for planargate devices to etch SiN at a power of 80/10 W until SiN was completely removed. Cl_2/BCl_3 mixed plasma was used for recessed-gate devices to etch InAlN at a power of 50/15 W. The PET process was performed for several recessed-gate devices: the interface was oxidized by O_2 plasma at 50/15 W power for 10 s, N_2 was used to purge for 1 min, and then the oxide layer was removed by BCl_3 plasma at 50/15 W power for 75 s. Finally, 445-nm Ni/Au metal was evaporated to serve as a T-gate. The crosssection of a scaled recess-gate InAlN/GaN HEMT is shown in Figure 1.

Figure 2 shows the comparison of the atomic force microscope (AFM) surface morphology of unetched, PET- and ICP-etched samples. The root mean square (RMS) indicates the roughness of the surface of the material. The larger the RMS, the more pronounced the undulation of the material surface and the higher the roughness. Large numbers of nanoparticles (black dots) are observed on the etched surface even after wet cleaning in organic solutions, resulting in an RMS roughness of 0.52 nm within the area of 8×8 μm^2. For the PET-etched samples, an RMS of 0.62 nm was obtained. The PET process can oxidize the surface of the material and etch the residue through low-power etching to ensure that the etched surface roughness is reduced and that the interface quality is improved. ICP etching treatment

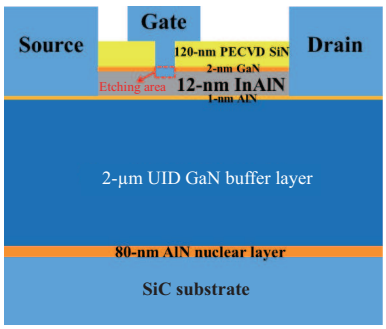

Figure 1 (Color online) Schematic cross-section of a recessed-gate InAlN/GaN HEMT.

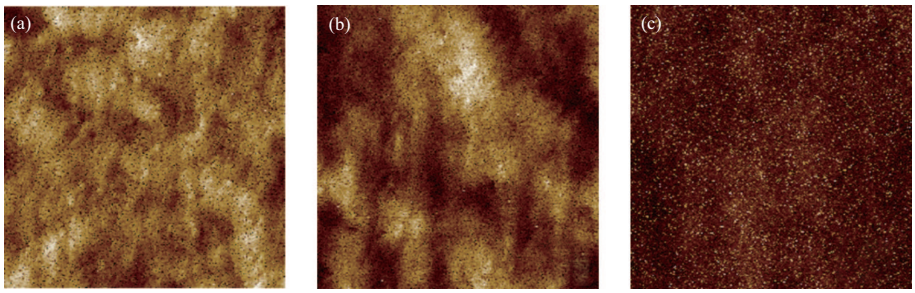

Figure 2 (Color online) AFM surface morphology (area: 8×8 μm^2) of InAlN/GaN samples (a) without ICP etching, (b) with ICP etching, and PET (c) with ICP etching.

resulted in an RMS value of 1.39 nm. The impact of high-energy particles caused large fluctuations on the surface of the material, increased the interface damage, and affected the reliability of the device.

3 Results and discussion

Three types of devices with different structures and conditions were designed: sample A is a planar-gate device without etching; sample B is a PET-etched recessed-gate device; and sample C is a recessed-gate device processed with ICP etching, respectively.

As shown in Figure 3, we extracted the transport properties of the device with the gate length L_g = 1 μm and L_{SD} = 7 μm under the drain bias of 5 V. The maximum saturation current of sample A is 1201.3 mA/mm, the peak trans-conductance is 224.9 mS/mm at V_d = 5 V. The maximum saturation currents of samples B and C were 1089.2 and 731.1 mA/mm, respectively. The peak trans-conductances of samples B and C were 299.9 and 170.7 mS/mm at V_d = 5 V, respectively. As the etching depth is increased, the saturation current of the device decreases, and the trans-conductance peak value increases, which is caused by the weakening of the polarization effect of the etched area. The close distance between the gate and the channel results in a more substantial gate control capability. After gate recess etching, the leakage of samples A and B increases. The recessed-gate etching makes the Inall barrier layer thinner, leading to a decrease in the distance between the gate and the 2DEG channel. This increases the tunneling probability of channel electrons that are under the action of a strong field. For sample B, although the recessed gate etching process was optimized, the bombardment of plasma caused inevitable damage to the InAlN barrier layer under the gate. The damage introduced leakage channels under the gate and increased the gate leakage current.

The transport properties of the recessed-gate device by ICP etching with PET were standard. However, the measured peak trans-conductance of the recessed-gate device by ICP etching is lower than that of the planar-gate device, which is an anomaly. As the etching depth of the recessed-gate device is increased, the ability to control the channel gate is further enhanced. The trans-conductance was obtained by the partial differentiation of the source and drain current with respect to the gate voltage. We speculate that this unusual phenomenon is caused by etching damage.

Considering the effect of the series resistance, the extrinsic trans-conductance $g_{m,\mathrm{ext}}$ of the device can

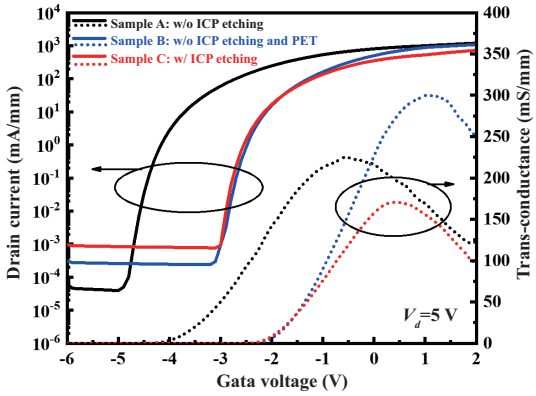

Figure 3 (Color online) Transfer curves of the planar-gate device (sample A), recessed-gate device by ICP etching with PET (sample B), and ICP etching (sample C).

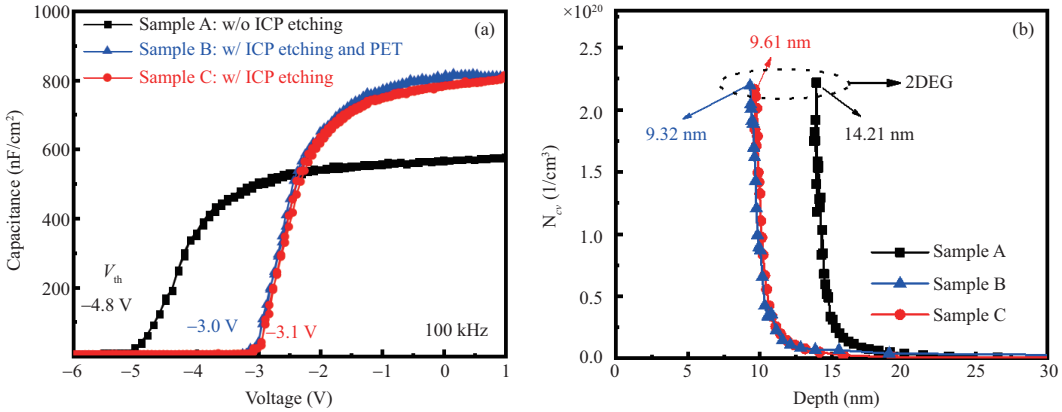

Figure 4 (Color online) (a) *C*-*V* characteristics at a frequency of 100 kHz: for sample A device without recessed gate and for samples B and C with recessed gate. (b) 2DEG distribution (N_{CV}) versus depth for samples A, B, and C.

be expressed as

$$g_{m,\mathrm{ext}} = \frac{g_{m,\mathrm{int}}}{1 + R_S \cdot g_{m,\mathrm{int}}}, \tag{1}$$

where $g_{m,\mathrm{ext}}$ is the extrinsic trans-conductance, $g_{m,\mathrm{int}}$ is the intrinsic transconductance, and R_S is the series resistance of source and gate. For a device with a short gate, the influence of the gate-source parasitic resistance R_S on the trans-conductance is not negligible. For long-gate devices, the channel resistance is still many orders of magnitude higher than the gate-source parasitic resistance R_S. Therefore, the measured trans-conductance did not increase as expected mainly because of the decrease in the intrinsic trans-conductance. The intrinsic trans-conductance of the device was determined by the field-effect mobility, electric field, and capacitance.

Figure 4(a) shows the *C*-*V* characteristics of three samples tested at a frequency of 100 kHz. The V_{th} of sample A is −4.8 V, and the thresholds of samples B and C are −3.0 and −3.1 V, respectively. The capacitance values of samples B and C are similar but greater than that of sample A. For recessed gate devices, the distance from the gate pin to the channel is reduced, and the capacitance is increased. The source-drain spacing of the same device is 26 μm and does not change. Thus, the electric field intensity between the source and the drain remains unchanged. The etching process will introduce some traps and impurities on the InAlN surface, and the field-effect mobility will be reduced because of the scattering effect [18]. Therefore, the decrease in the intrinsic trans-conductance is caused by the reduction in mobility.

Using equations $\mathrm{Depth} = \frac{\varepsilon_r \varepsilon_0}{c}$ and $N_{CV} = -\frac{1}{Q\varepsilon_r\varepsilon_0} \times \frac{1}{\frac{\mathrm{d}c^{-2}}{\mathrm{d}V}}$, the relationship between the carrier concentration in recessed-gate and the depth can be obtained from the differentiation of the *C*-*V* curve. Here, N_{CV} is the carrier concentration at the corresponding depth, ε_r is the relative permittivity of the barrier layer and the insulating layer, and ε_0 is the vacuum permittivity. As shown in Figure 4(b), for the three samples, we detected the N_{CV} of different depths under the gate by the measured capacitance

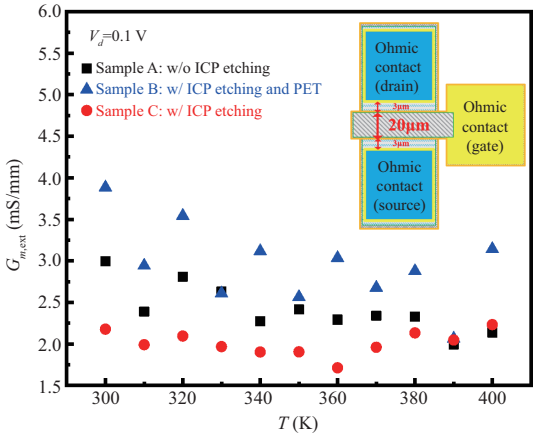

Figure 5 (Color online) Top view of the devices and perform variable temperature (T) test on samples A, B, and C.

and determined the position of 2DEG. The thickness of the barrier layer is 9.32 nm for sample B. This value is 4.89 nm smaller than 14.21 nm in the unetched area. For sample C, the height of the barrier layer is 9.61 nm, which is similar to that of sample B. This is equivalent to the etch depth of the expected design. The polarization effect and strain of the devices may differ because the three samples have varying architectures and circumstances. The in-strain in the device without PET and with PET varies from -0.0215 to -0.0219 after computation, which has minimal effect on the transport characteristics of the device. Compared with sample A, the in-strain of samples B and C decreases by 9.7% and 11.7%, respectively. Sample B has a 1.8% decrease relative to sample C.

As shown in Figure 5, the DC test was performed on a device with a gate length of 20 μm. The devices were tested in the temperature range of 300–400 K with a step of 10 K, and its maximum trans-conductance point was tested at $V_d = 0.1$ V. As the temperature increases, the top trans-conductance points of samples A and B gradually decrease. We believe that this is because the optical phonon scattering mechanism affects the field-effect mobility of the device after the temperature is increased, and the trans-conductance continues to decrease. For sample C, as the temperature changes, the trans-conductance is almost always in a relatively balanced state, confirming that the recess damage introduced by dry etching is considerable. Thus, the main reason for the change in the original scattering mechanism of the sample is the decrease in the effect of the optical phonon scattering mechanism. It is dominated by another mechanism not related to temperature. At this time, the long-distance impurity scattering of channel electrons dominates the scattering mechanism. The long-range impurity scattering mechanism does not change with temperature. That is, the trans-conductance does not change with temperature. We calculate that the field-effect mobility of sample A is 1155.3 $\mathrm{cm^2/V \cdot s}$, and that of sample B is 1075.5 $\mathrm{cm^2/V \cdot s}$, slightly lower than that of sample A, which is a logical phenomenon. The field-effect mobility of sample C is 699.1 $\mathrm{cm^2/V \cdot s}$. This confirms the previous speculation in this paper: the intrinsic trans-conductance is mainly affected by the field-effect mobility. The drift velocity of three samples is also analyzed. In the linear region, we calculated the electron drift speeds in 300 K of samples A, B, and C as 1.65×10^6, 1.54×10^6, 9.99×10^5 cm/s, respectively. The electron drift speed of sample C is significantly lower than those of samples A and B, which is caused by a decrease in the electron drift velocities due to the scattering by imperfections (interface roughness, dislocations, etc).

For polar semiconductors such as nitrides, the carrier mobility is mainly affected by remote charge scattering (REM) and optical phonon scattering (PO) [19]. When the ambient temperature is higher than 200 K, the field-effect mobility of the Schottky gate heterostructure is mainly dominated by optical phonon scattering [20]. Polar optical phonon scattering is inelastic scattering. The mobility of devices decreases significantly with increasing temperature. As shown in Figure 6, the simulation of the scattering mechanism with temperature for the device with $N_s = 10^{13}$ $\mathrm{cm^{-2}}$ through MATLAB shows that the optical phonon scattering mechanism decreases as the temperature is increased. This is because the optical phonon scattering causes the lattice atoms to vibrate away from their lattice points. At this time, the electric field is locally destroyed, causing the electrons to move in the direction of segregation. As the temperature is increased, the energy of the electrons affected by the scattering effect changes, and its effective mass also changes. The mobility changes accordingly. As for the REM scattering mechanism, its influence on the mobility does not change with temperature. ICP etching can cause damage to the

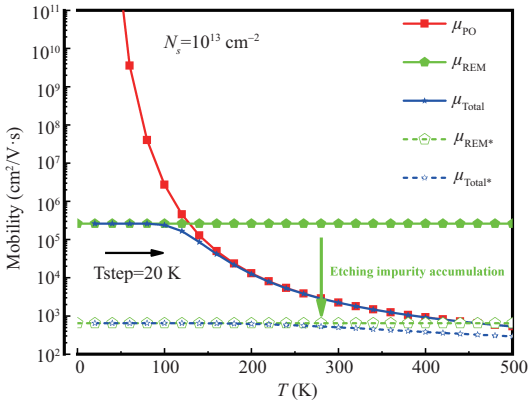

Figure 6 (Color online) Relationship of the scattering mobility and temperature when the 2DEG density is 1.0×10^{13}cm^{-2}.

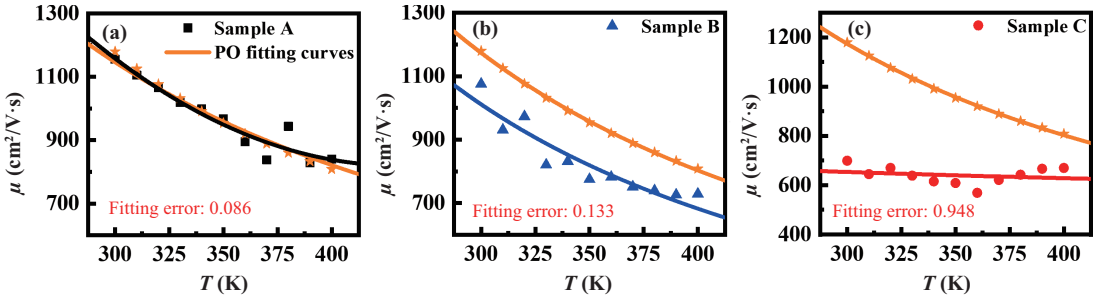

Figure 7 (Color online) Statistical peak field-effect mobility of (a) sample A, (b) sample B, and (c) sample C as a function of temperature (geometries) and fit curves by using the optical phonon scattering model (lines).

recess of devices. The etching damage is mainly manifested in the increase in the interface roughness. This is because as the high-energy particles continue to bombard the surface, some by-products produced by physical bombardment and chemical action will continue to roll in the recess. The product forms a magazine layer. The presence of this impurity layer will lead to an enhanced REM scattering mechanism. As the impurity layer accumulates, the effect of the REM scattering mechanism will reduce mobility. According to the formula in the figure, it can be seen that when the impurity layer accumulates to a certain level, the REM scattering mechanism will exceed the PO scattering mechanism and become the dominant factor for the decline in mobility. Low-temperature experiments and the results of the simulation are identical. At a temperature above 120 K, the mobility of samples A and B begins to decrease, whereas that of sample C remains almost unchanged.

The numerical simulation shows an exponent-like dependence of mobility on T, revealing the dominant mechanism of optical phonon scattering, which is expressed as [21]

$$\mu = \frac{qh}{4\pi m^* E_l \alpha}\left[\exp\left(\frac{E_l}{kT}\right) - 1\right]\varphi, \tag{2}$$

where h is the Plank constant, m^* is the effective mass of the electron, E_l is the optical phonon energy, and α is the Fröhlich constant. At high temperatures, the coefficient φ is expressed as $(8/3)\cdot(kT/\pi E_l)^{1/2}$. The temperature-dependent peak field-effect mobility is plotted in Figure 7. The fitting errors of samples A, B, and C relative to the standard are 0.086, 0.133, and 0.948, respectively. The dependence of mobility on the temperature is determined by the combination of the effective mass and optical phonon scattering energy. The channel electrons of each sample are scattered by the PO mechanism and the REM mechanism. Samples A and B have a higher degree of fitting, and the optical phonon scattering mechanism dominates the decrease in mobility. The fitting result of sample C is unusual. This is due to the fact that ICP etching introduces many impurities in the recess, which enhances the remote charge scattering effect. At this time, the channel electrons are mainly affected by the REM scattering mechanism.

The expression for the remote scattering rate using a self-consistent wave function can be derived from

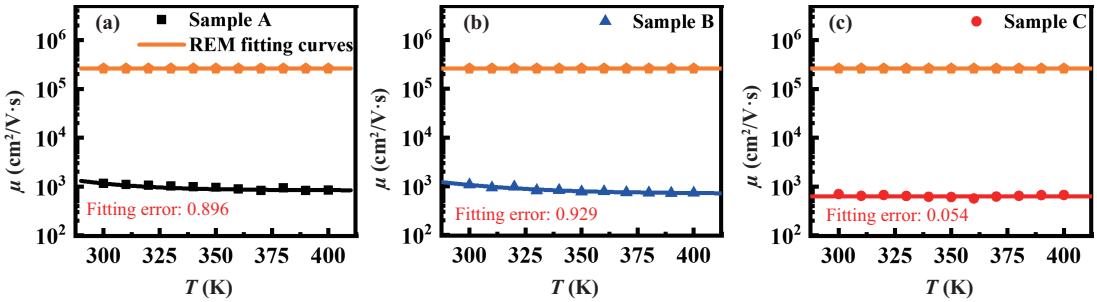

Figure 8 (Color online) Statistical peak field-effect mobility of sample A (a), sample B (b), and sample C (c) as a function of temperature (geometries) and fit curves by using the remote charge scattering model (lines).

Fermi's golden rule as follows:

$$\frac{1}{\tau_{\mathrm{REM}}} = n_{\mathrm{fix}} \frac{m^*}{2\pi\hbar^3 k_F^3} \int_0^{2k_F} |V_{nm}(q)|^2 \frac{q^2 \mathrm{d}q}{\sqrt{1-(\frac{q}{2k_F+q_{TF}})^2}}, \tag{3}$$

where n_{fix} is the interface charges destiny and k_F and q are the Fermi wave factor and the wave factor, respectively. The distance between 2DEG and the dielectric/InAlN interface is d; un and um are the wave functions of the initial and final subbands, respectively. This equation is related to the thickness of the barrier layer and the interface charge density, demonstrating that the remote charge scattering mechanism grows stronger as the barrier layer thickness is reduced or the interface charge density is increased. The temperature-dependent peak field-effect mobility is plotted in Figure 8. The fitting errors of samples A, B, and C relative to the standard are 0.896, 0.929, and 0.054, respectively, which corresponds to the conclusion of Figure 7. Samples B and C have the same etching depth; thus, their barrier thickness is the same. ICP etching introduces impurities in the recess, which increases the interface charge density and enhances the REM scattering effect. This process is clearly responsible for sample C.

4 Conclusion

In this study, the electrical transport properties of planar- and recessed-gate InAlN/GaN HEMTs were comparatively analyzed. Compared with the device manufactured using ICP etching, the PET-etched device has lower etching damage and better transport properties. It should be noted that the reduction in the intrinsic trans-conductance of the recessed-gate devices is related to the mobility of the devices. After conducting a variable temperature test, we concluded that the change in the scattering mechanism caused this phenomenon. The damage from ICP etching leads to an increase in the interface charge density, and the remote charge scattering mechanism dominates the photon scattering mechanism, which is the main reason that affects the transmission characteristics of the embedded gate device. Furthermore, we verified the process of the accumulation of etching impurities and the remote charge scattering mechanism as the primary scattering mechanism through a simulation. For the PET-etched device, this method can effectively reduce the damage of the etching interface, prevent the accumulation of impurity layers, effectively improve the performance of InAlN/GaN HEMTs, and provide an alternative for the development of high-frequency and high-power devices.

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References

1 Millan J, Godignon P, Perpina X, et al. A survey of wide bandgap power semiconductor devices. IEEE Trans Power Electron, 2014, 29: 2155–2163
2 Jones E A, Wang F F, Costinett D. Review of commercial GaN power devices and GaN-based converter design challenges. IEEE J Emerg Sel Top Power Electron, 2016, 4: 707–719
3 Mi M H, Wu S, Yang L, et al. In-situ SiN combined with etch-stop barrier structure for high-frequency AlGaN/GaN HEMT. Chin Phys B, 2020, 4: 430–433
4 Jessen G H, Fitch R C, Gillespie J K, et al. Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices. IEEE Trans Electron Device, 2007, 54: 2589–2597
5 Saito W, Takada Y, Kuraguchi M, et al. Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications. IEEE Trans Electron Device, 2006, 53: 356–362

6 Shen L, Coffie R, Buttari D, et al. High-power polarization-engineered GaN/AlGaN/GaN HEMTs without surface passivation. IEEE Electron Device Lett, 2004, 25: 7–9
7 Yang J C, Ahn S, Ren F, et al. Inductively coupled plasma etch damage in (−201) Ga_2O_3 Schottky diodes. Appl Phys Lett, 2017, 110: 142101
8 Lebreton F, Abolmasov S N, Silva F, et al. In situ photoluminescence study of plasma-induced damage at the a-Si:H/c-Si interface. Appl Phys Lett, 2016, 108: 051603
9 Hiblot G, van der Plas G. Factor analysis of plasma-induced damage in bulk FinFET technology. IEEE Electron Device Lett, 2018, 39: 927–930
10 Koretomo D, Toda T, Matsuda T, et al. Anomalous increase in field-effect mobility in In-Ga-Zn-O thin-film transistors caused by dry-etching damage through etch-stop layer. IEEE Trans Electron Device, 2016, 63: 2785–2789
11 Zhang Y C, Huang S, Wei K, et al. Millimeter-wave AlGaN/GaN HEMTs with 43.6% power-added-efficiency at 40 GHz fabricated by atomic layer etching gate recess. IEEE Electron Device Lett, 2020, 41: 701–704
12 Jing S Q, Ma X H, Zhu J J, et al. Interface and border trapping effects in normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs with different post-etch surface treatment. Chin Phys B, 2020, 29: 531–535
13 Zhu J J, Jing S Q, Ma X H, et al. Improvement of electron transport property and on-resistance in normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs using post-etch surface treatment. IEEE Trans Electron Device, 2020, 67: 3541–3547
14 Wang Y, Wang M J, Xie B, et al. High-performance normally-off Al_2O_3/GaN MOSFET using a wet etching-based gate recess technique. IEEE Electron Device Lett, 2013, 34: 1370–1372
15 Lin J, Antoniadis D A, del Alamo J A. Off-state leakage induced by band-to-band tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs. IEEE Electron Device Lett, 2014, 35: 1203–1205
16 Gao J N, Jin Y F, Xie B, et al. Low ON-resistance GaN Schottky barrier diode with high V-ON uniformity using LPCVD Si_3N_4 compatible self-terminated, low damage anode recess technology. IEEE Electron Device Lett, 2018, 39: 859–862
17 Fernández-Garrido S, Gačević Z, Calleja E. A comprehensive diagram to grow InAlN alloys by plasma-assisted molecular beam epitaxy. Appl Phys Lett, 2008, 93: 191907
18 Wang R H, Saunier P, Xing X, et al. Gate-recessed enhancement-mode InAlN/AlN/GaN HEMTs with 1.9-A/mm drain current density and 800-mS/mm transconductance. IEEE Electron Device Lett, 2010, 31: 1383–1385
19 Sze S M, Ng K K. Physics of Semiconductor Devices. 3rd ed. Hoboken: Wiley, 2007
20 Wang M T, Cheng B Y Y, Lee J Y. Temperature-dependent degradation mechanisms of channel mobility in ZrO_2-gated n-channel metal-oxide-semiconductor field-effect transistors. Appl Phys Lett, 2006, 88: 242905
21 Fröhlich H. Electrons in lattice fields. Adv Phys, 1954, 3: 325–361