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• **Supplementary File** •

Insights of V_G-dependent threshold voltage fluctuations from dual-point random telegraph noise characterization in nanoscale transistors

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Appendix A Basic device performances

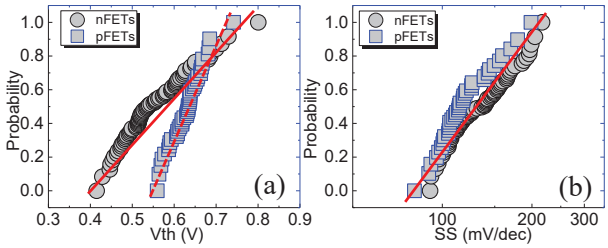

Figure A1 The distribution of (a) Threshold Voltages (normal) and (b) Subthreshold Swing (lognormal) for nFETs and pFETs, respectively.

Both nMOS and pMOS high-κ planar transistors are measured with the channel length of 70nm, the channel width of 90 nm and the equivalent oxide thickness of 1.65 nm. All the measurements are conducted at room temperature with a drain voltage of 100 mV by using a commercial semiconductor analyzer. A standard fast configuration connection is adopted, in which two pulse units are connected with the Gate and Drain while the Source and Substrate are grounded. The distributions of the threshold voltage (Vth) and subthreshold swing (SS) for both nFETs and pFETs are displayed Fig. A1(a) and Fig. A1(b), respectively. The Vths of devices are extracted by using the max transconductance method, and the SS values are from the slope values of the linear fitting between V_G and log10(I_D). The Vths exhibit normal distributions for nFETs (guided by solid line) and pFETs (guided by dash line), respectively. It is vivid to see that the Vths of nFETs are more scattered than that of pFETs. Moreover, the SS values of pFETs are relatively smaller than that of nFETs, both of which are following a lognormal distribution guided by the red line. This indicates that the measured devices exhibit similar interface properties and device performances.

Appendix B Vg dependent threshold voltage fluctuations

The RTN trap induced multi-level $I_D - V_G$ curves are measured with the dielectric trap frozen in its charged or empty state, which is explained in detail in our previous work [1, 2]. Without a tough selection on the measured devices, a broad range of transfer curve can be experimentally measured, in which the obvious and large fluctuations can help distinguish the unobvious fluctuations out of the measurement window. Moreover, the two-level and four-level transfer curves are reported to be obtained from the nanoscale transistors with single trap and double traps, respectively. Therefore, the RTN magnitudes can be extracted for an entire gate-voltage range from the subthreshold to the linear region, including drain current fluctuations (ΔI_D) and threshold voltage fluctuations (ΔVth). The $\Delta Vth0$ and $\Delta VthH$ are defined (guided by the white arrows) as the threshold voltage fluctuations ($\Delta Vths$) around the threshold region ($V_G - V_{th0}$=0.0V) and the linear

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region ($V_G - V_{th0}$=0.5V), respectively. Noted that the defined $\Delta Vth0$ could avoid the discussion on the complex conditions caused by the random distributed percolation paths, which can inevitably lead to device-to-device variations, especially in the subthreshold region. Therefore, the investigation mainly focuses on the threshold region ($\Delta Vth0$) and above ($\Delta VthH$). Noted that all the measurements and extractions are conducted under the same conditions. Moreover, the initial device performances are found to have ignorable impacts on the observed trends in Fig. 1(c). At least 15 devices are taken to calculate each auto-correlation coefficient for reducing the statistical errors. Before the calculation, the measured devices are divided into several groups depending on whether their $\Delta Vth0s$ are larger than certain values. Therefore, there is only one group for the devices whose $\Delta Vth0$ is larger than 5 mV.

Appendix C RTN trap distributions

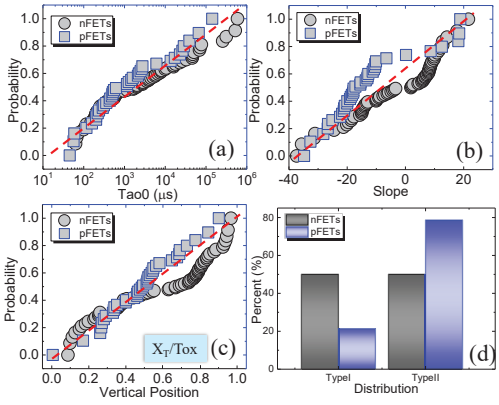

Figure C1 The distribution of (a) $\tau 0$ (intersection value of τ_c-V_G line and τ_e-V_G lines), (b) slope ($\tau c/\tau e$ versus V_G curve), and (c) RTN trap vertical position in the dielectric layer for nFETs and pFETs, respectively. (d) The histogram of RTN types (TypeI: carriers exchange between trap and channel; TypeII: carriers exchange between trap and gate) for nFETs and pFETs, respectively.

The RTN trap position in the vertical direction of the dielectric layer is evaluated by using the following equation:

$$\frac{X_T}{T_{ox}} = -\frac{kT}{q}\frac{\partial ln(\tau_c/\tau_e)}{\partial V_G}(1),$$

where Tox is the equivalent oxide thickness, k is Boltzmann constant, T is temperature and q is the elementary charge [3,4]. The statistic results on the trap vertical locations are displayed in Fig. C1(c) with a similar normal distribution, which also indicates uniform characteristics for the measured devices. Moreover, the RTN traps are located nearer to the gate electrode for pFETs than that of nFETs. Normally, the RTN traps are categorized as Type-I and Type-II, which exchange carriers with the conducting channel (positive slope) and the gate electrode (negative slope), respectively. For Type-I traps, the vertical positions could be extracted directly from equation (1). When comes to Type-II traps, the extracting equations are modified as:

$$\frac{T_{ox} - X_T}{T_{ox}} = \frac{kT}{q}\frac{\partial ln(\tau_c/\tau_e)}{\partial V_G}(2).$$

According to the histogram in Fig. C1(d), Type-I and Type-II traps are roughly equal (∼49.3%:50.7%) for nFETs, while the ratio turns to be ∼ 84.2%:15.8% for pFETs. Moreover, Type-I traps are more likely to be located closer to the channel, whereas Type-II traps are basically closer to the gate in nFETs. When comes to pFETs, Type-II traps dominate with a roughly Gaussian distribution. In the sub-threshold region, a larger threshold voltage fluctuation is normally coming from the RTN traps nearer to the channel, in which the random percolation paths induced electric potential fluctuations enhance the RTN magnitudes. Above the threshold voltages, the RTN magnitudes can be ascribed to the mobility ($\Delta\mu$) fluctuation model and carrier number (Δn) fluctuation model. For the Type-I (dielectric-channel) traps, both $\Delta\mu$ and Δn models should be considered, while for the Type-II RTN traps, the $\Delta\mu$ model is the dominant factor in fluctuation as the dielectric-gate interactions have limited impacts on the number fluctuation. Approaching the operating conditions, the distributions of the $\Delta Vths$ becomes narrow, since a larger V_G makes the multiple percolation paths combining into a whole current channel. RTN traps are likely to be located closer to the gate in pFETs (Type-II dominant), which could lead to a relatively strong control ability for the V_G on the drain current showing smaller SS values and larger transconductance. Meanwhile, it seems that the percolation paths disappear faster in nFETs than that in pFETs, resulting in the different relationship between V_G and threshold voltage fluctuations.

Appendix D Generation method of V_G dependent ΔVth

The flowchart of the proposed method to generate V_G dependent $\Delta Vths$ is shown in Fig. D1. Firstly, the distributions of the threshold voltage fluctuations at the threshold voltage and operating voltage are analyzed, which all follow the log-normal

distributions. The statistics parameters including the mean value and the variance of $\Delta Vth0$ and $\Delta VthH$ are extracted for both nFETs and pFETs, respectively (Step-I). By using the mean value and the variance of the measured $\Delta Vth0$, a random number generator is adopted to generate the multiple $\Delta Vth0s$ (100 samples), which can also follow the similar log-normal distributions (Step-II). Secondly, the experimentally measured RTN magnitudes ($\Delta Vth0$ and its corresponding $\Delta VthH$) are divided into several groups under different $\Delta Vth0s$ with a step of $\sim$ 1.0 mV (Step-III). For instance, all the devices whose $\Delta Vth0s$ are in the range from 0.0 mV to 1.0 mV are classified into one group (the average 0.5 mV group). Thirdly, in each group, the mean value (black squares) and the variance (red circles) of the measured $\Delta VthH$ are extracted and plotted under various $\Delta Vth0$ from 0.5 mV to $\sim$ 10 mV (Appendix D, Fig. D2) for nFETs and pFETs, respectively. Then the scatter points are fitted with a lognormal distribution guided by the black and red dash line, which indicates the distributed parameters of the $\Delta VthH$ could be obtained for any given $\Delta Vth0$ (Step-IV). Finally, each generated $\Delta Vth0$, following the log-normal distribution (according to Step-I), could get its corresponding $\Delta VthH$ with the statistic parameters (obtained from the fitting trends in Step-IV).

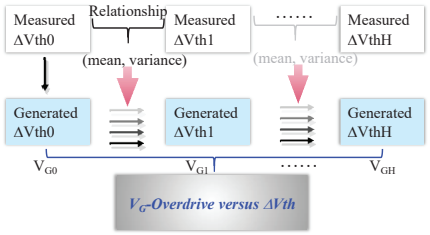

Figure D1 The flowchart to generate various $\Delta VthH$ values from the measured data for simulating the V_G dependent threshold voltage fluctuations.

Fig. D2 shows the statistical information of the measured $\Delta VthH$ (a&d), generated and measured $\Delta VthH$ (b&e), and relationship between generated $\Delta Vth0$ and $\Delta VthH$(c&f) for nFETs and pFETs, respectively. Moreover, the accurate distribution parameters and dependent relationships are important for obtaining a smoother V_G-ΔVth curve, which normally requires a large number of measured devices. To demonstrate the generation processing, only two gate voltages are adopted, which are corresponding to $V_G - V_{th0}$ =0.0 V and V_G-V_{th0} =0.5 V, respectively. By using different voltage steps like V_{G1}, V_{G2}, etc., a full range of V_G dependent ΔVth could be obtained following the generation flowchart, which is beneficial in the RTN aware circuit simulation and design.

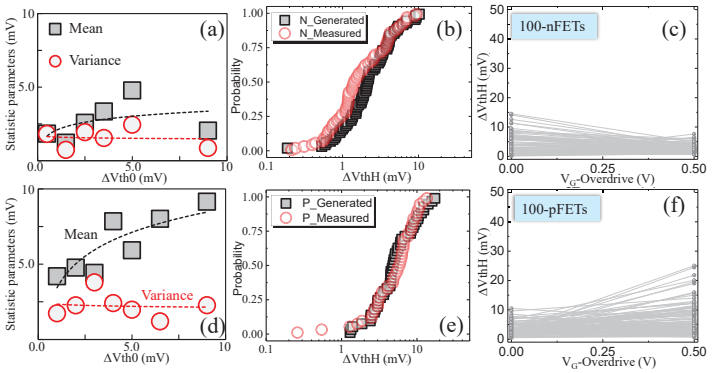

Figure D2 (a&d) Log-normal modeling to extract mean values and variances with different ΔVth0; (b&e) Log-normal distribution of the experimental and generated ΔVthH; (c&f) 100 generated V_G dependent RTN magnitudes for nFETs and pFETs, respectively.

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