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Single event transients induced by pulse laser in Ge pMOSFETs and its supply voltage dependence

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Dear editor,

Germanium (Ge) has been considered as a promising candidate of channel material for sub-7 nm owing to its high carrier mobility and good compatibility with conventional Si CMOS process [1]. Although Ge-based technology is still under development and not in massive production, it is quite meaningful to explore its single event effect (SEE) before potential space applications.

Single event transient (SET) is one of the most important SEEs in device-level research. Compared with silicon, germanium has very different physical and electrical properties which may significantly impact SET response. Until now, there are limited reports focusing on the SET response of Ge MOSFETs. SiGe MOSFETs with ultra-thin quantum well (QW) channels and Ge channel pMOSFETs based on Si substrate demonstrate similar polarity dependence of SET on the strike location [2, 3], which has never been observed in Si MOSFETs. However, the unique polarity dependence is mainly due to its special device structure. Therefore, to further understand the basic mechanism of SET in Ge-based MOSFETs, it is necessary to experimentally study the SET response of Ge MOSFETs with conventional device structure.

Besides, supply voltage plays an important role in the power consumption of integrated circuits (ICs). Reducing the supply voltage is beneficial for low power applications. However, the decrease of supply voltage can cause the enhanced single event vulnerability in Si-based technology, which has been experimentally illustrated in previous work [4]. Yet the supply voltage dependence of SET in Ge MOSFETs is still unknown, which is worthy to be investigated.

In this study, the pulse laser induced SET in bulk Ge pMOSFETs is experimentally investigated. The most sensitive incident location is illustrated. Further, the supply voltage dependence of transient currents in Ge pMOSFETs is experimentally evaluated and compared with Si pMOSFETs. The results offer early insight into the basic mechanism of SET response in Ge MOSFETs, which may provide guidance for the radiation-hardened design of novel Ge-based ICs for aerospace applications.

The devices under test (DUTs) are planar pMOSFETs fabricated on bulk Ge wafer [5]. The gate length and gate width of DUTs are 10 and 20 μm, respectively. All DUTs are unpackaged and real-time tested on the wafer.

Single photon absorption (SPA) pulse laser experiments are performed at National Space Science Centre in Chinese Academy of Sciences. The laser beam is focused on the topside of DUTs, and a 50x microscope objective is used to create a spot size of 2–3 μm. The laser pulse with wavelength of 1064 nm and pulse width of 30 ps is used. The Ge pMOSFETs are biased in off-state. Specifically, the drain is biased at −0.8 V with source, gate and substrate grounded.

Figure 1(a) shows the drain currents induced by laser with the energy of 311 pJ as a function of time at different strike locations. The position 0 μm is defined when the laser is focused on the edge of the source and the position 30 μm stands for the edge of the drain, as shown in the inset of Figure 1(a). From Figure 1(a), the magnitude of drain current struck at the position of 22 μm, corresponding to the drain region of Ge pMOSFETs, is significantly larger than in other cases. The case of drain strike shows the largest collected charges. The peak current gradually increases as the strike location moves from source to drain, then suddenly decreases because of the metal covering the drain region ($X > 22$ μm). Considering both peak current and collected charges, the drain region is the most sensitive incident location for bulk Ge pMOSFETs, which is similar to planar bulk Si MOSFETs [6]. This result can be explained by the high electric field at the drain region. For the case of the drain strike, laser induced charges under the drain region can be collected immediately through the drift process by the electric field of the p-n junction between drain and substrate, which leads to a large number of collected charges and a high transient current. However, once the incident location is outside the drain region, charges induced inside Ge pMOSFET need to transport to the p-n junction through the diffusion process and then be collected by the

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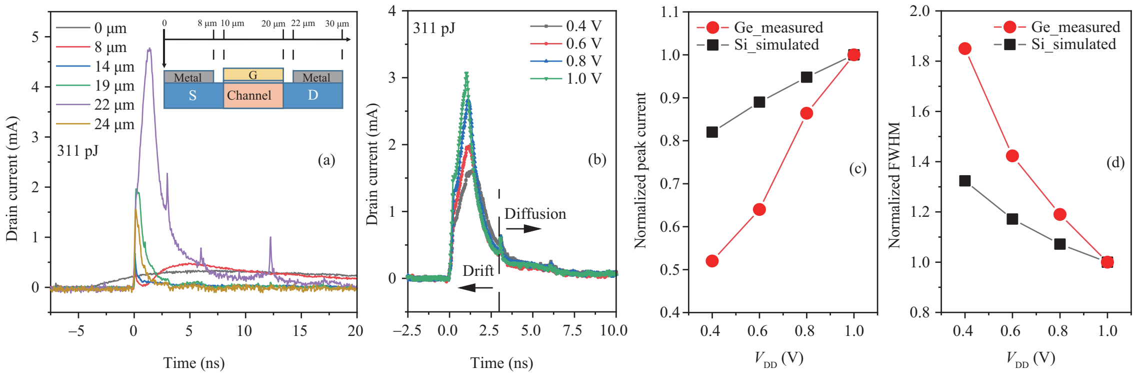

Figure 1 (Color online) Drain currents induced by laser as a function of time (a) at different strike locations and (b) under different supply voltages. The inset shows the relative position of laser strikes. The comparison of (c) peak current and (d) pulse width as the function of supply voltage between Ge pMOSFETs and Si pMOSFETs.

drain. During the diffusion process, recombination of excess carriers occurs, resulting in a smaller amount of collected charges and lower transient current.

Furthermore, the polarity of transient current shown here is not affected by the strike location, different from polarity dependence results reported previously [2, 3]. In our study, the conventional planar bulk structure is used and no polarity dependence is observed. So the polarity dependence observed previously is not attributed to the Ge material.

Further, the supply voltage dependence of SET in Ge pMOSFETs is experimentally evaluated. Figure 1(b) illustrates the drain currents of Ge pMOSFETs under different supply voltages. As shown in Figure 1(b), a significant difference is observed for the transient currents corresponding to the drift process, but the transient tails representing the diffusion process are almost the same. Supply voltage mainly affects the electric field at the drain region, thus it can be expected that when charges are transported toward the drain by the drift process, the carrier velocity decreases with supply voltage reduction. When supply voltage reduces from 1.0 to 0.4 V, the peak current of transients decreases. The pulse width is defined as the full width at half maximum (FWHM) of transient current. The pulse width of transients of Ge pMOSFETs increases with supply voltage down-scaling.

To compare the supply voltage dependence of SETs between Ge pMOSFETs and Si counterparts, 3D TCAD simulation is carried out. A Si pMOSFET with the same structural parameters as Ge devices is developed in Sentaurus for comparison. The HeavyIon model is used to simulate the ion strikes. The comparison of peak current and pulse width between Ge and Si pMOSFETs are shown in Figures 1(c) and (d), respectively. All data are normalized to the respective value corresponding to 1.0 V. The peak current and pulse width of Ge pMOSFETs change more remarkably with supply voltage compared with Si devices. As supply voltage reduces from 1.0 to 0.4 V, the peak transient current for Ge pMOSFETs decreases by 48%, while 18% decreases for Si devices. The pulse width of transient current for Ge pMOSFETs increases by 85%, while 32% increases for Si counterparts.

When the supply voltage reduces, the carrier velocity of Ge and Si decreases due to the decrease of the electric field. However, the carrier velocity of Ge pMOSFETs is relatively more sensitive to electric field compared with Si. Therefore, supply voltage has a more significant effect on peak current and pulse width in Ge pMOSFETs. The results imply that supply voltage has a much larger impact on SET in Ge pMOSFETs. More vulnerable SET response of Ge MOSFETs at low supply voltage may bring more challenges to the radiation-hardened design of Ge-based ICs.

Summary. The SETs of bulk Ge pMOSFETs are experimentally investigated through pulse laser irradiation. The higher peak current and the larger amount of collected charges are observed when the laser focuses on the drain region, indicating that the drain region is the most sensitive incident location for bulk Ge pMOSFETs. Moreover, the supply voltage dependence of transient in Ge pMOSFETs is investigated and compared with Si counterparts. Transient currents of Ge pMOSFETs change more significantly with supply voltage scaling compared with Si pMOSFETs. The more vulnerable SETs of Ge pMOSFETs at low supply voltage should be taken into consideration for the radiation-hardened design of Ge-based ICs.

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