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Novel SiC SBD-wall-integrated trench MOSFET with a semi-superjunction and split trench gate

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Dear editor,

SiC MOSFET has the advantages of low specific on-resistance ($R_{\rm on,sp}$), high breakdown voltage (BV), high operating temperature, and low thermal resistance. As a switching device, SiC MOSFET needs an anti-paralleled freewheeling diode (FWD) in many cases. Owing to the wide band gap, the body diode in SiC MOSFET has a drawback of high turn-on voltage (V_F) in the reverse conduction [1]. Compared with the external Schottky barrier diode (SBD), an integrated SBD reduces extra package cost and stray inductance [2]. The superjunction (SJ) MOSFET can optimize the trade-off relationship between $R_{\rm on,sp}$ and BV, as well as reduce the switching loss by decreasing the gate-to-drain capacitance ($C_{\rm GD}$). However, the superjunction causes a large reverse recovery charge ($Q_{\rm rr}$) and a large reverse recovery current ($I_{\rm rr}$) during switching transients [3]. Meanwhile, the fabrication of SiC full superjunction is hard to realize on the condition of long deep N/P pillar [4].

A novel SiC SBD-wall-integrated MOSFET with a semi-superjunction (SSJ) and split trench gate (STG), called S^3-TMOS, is proposed. Static and dynamic characteristics are compared among the S^3-TMOS, SBD-wall-integrated trench MOSFET (SWITCH-MOS, S-MOS) [5] and conventional trench MOSFET (C-TMOS) by Sentaurus TCAD. Figure 1 shows the half-cell cross-sectional schematic performances of three devices and summarizes the performances from simulation. Compared with the other two devices, S^3-TMOS has superior static and dynamic performances.

Device structure and mechanism. The S^3-TMOS features a wall-integrated SBD, a semi-superjunction structure, and a split trench gate. First, the wall-integrated SBD on the side of the source trench provides a reverse conducting path as an FWD, which is turned on earlier than the body PN junction. Thus, the S^3-TMOS could achieve a low turn-on voltage V_F in the reverse conduction. Meanwhile, the SBD integrated in the side wall saves the device area. Second, the semi-superjunction structure optimizes the electric field (E-Field) distribution and allows a high N type drift doping concentration to achieve an ultralow $R_{\rm on,sp}$ with a high BV. In the S^3-TMOS, the $Q_{\rm rr}$ is decided by the depletion capacitance of the SBD and PN junction of SJ region in parallel, of which the capacitance of the PN junction is dominant owing to its much larger junction area. Furtherly, the PN junction area of the semi-SJ is smaller than that of full-SJ, and thus its $Q_{\rm rr}$ is smaller. Thus, we adapt the semi-SJ MOSFET to achieve a low $Q_{\rm rr}$ and reduce fabrication difficulty. Third, the split trench gate is located under the poly gate and shorted to the source electrode, so part of the $C_{\rm GD}$ could be transferred to drain-to-source capacitance ($C_{\rm DS}$). Therefore, the S^3-TMOS achieves lower $C_{\rm GD}$ and gate-to-drain charge ($Q_{\rm GD}$), and thus a lower switching loss. Fourth, the P-Shield region beneath the gate trench is immune to premature breakdown by avoiding punching through and shielding the trench gate from the high E-Field [6]. It also shapes a Junction-Barrier-Schottky (JBS) structure along with P-Body to inhibit the leakage current induced by the SBD. Multiple epitaxy plus ion implantation is adopted to obtain semi-superjunction structure. The formation of the split gate is realized by refill and patterned re-etch process. Ni single ohmic/Schottky contact process scheme is chosen in the metallization process to form the Schottky contact and ohmic contact at the same time.

Results and discussions. The S^3-TMOS owns the highest BV of 1604 V because the semi-superjunction structure introduces almost rectangular E-Field distribution rather than triangular E-Field distribution of the C-TMOS. Owing to a higher doping concentration in the drift region, the S^3-TMOS has much lower $R_{\rm on,sp}$ of 1.54 mΩ·cm^2 than those of the other devices and thus achieves the lowest static loss. The current spread layer (CSL) leads to a smaller $R_{\rm on,sp}$ of S-MOS than that of C-TMOS. Since the integrated SBD turns on earlier than the PN junction, both the S^3-TMOS and S-MOS have a very low V_F at reverse conduction cur-

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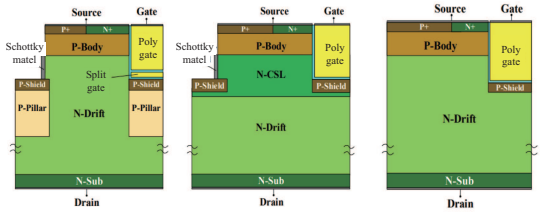
Structures			
	S^3-TMOS	S-MOS	C-TMOS
BV (V)	1604	1537	1357
$R_{on,sp}$ (mΩ·cm^2)	1.54	2.92	3.62
FOM (GW/cm^2)	1.67	0.81	0.51
V_F (V)	1.56	1.57	2.71
C_{GD} (pF/cm^2)	45.6	73.8	176.6
Q_{GD} (nC/cm^2)	166.6	248.6	417.3
E_{switch} (mJ/cm^2)	2.25	2.64	7.59

Figure 1 (Color online) Device structures and performance comparison of three devices.

rent of 100 A/cm^2. Furthermore, the S^3-TMOS has a low leakage current because of the narrowed path of leakage current caused by SSJ structure and JBS region. Thus, the S^3-TMOS could achieve higher reliability compared with S-MOS.

Dynamic characteristics of the three devices are also discussed. The STG transfers part of C_{GD} to C_{DS}, and thus the C_{GD} of the S^3-TMOS is 38% and 74% lower than that of S-MOS and C-TMOS, respectively. The S^3-TMOS exhibits the lowest Q_{GD} of 166.6 nC/cm^2, which is much lower than 417.3 nC/cm^2 of C-TMOS and 248.6 nC/cm^2 of S-MOS. Owing to the lower C_{GD} and Q_{GD}, higher dV/dt and dI/dt values can be achieved in S^3-TMOS, resulting in a lower switching loss. The switching loss (E_{switch}) of S^3-TMOS is 2.25 mJ/cm^2, which is 15% and 70% lower than that of S-MOS and C-TMOS, respectively. Meanwhile, the S^3-TMOS maintains almost the same voltage/current overshoot in spite of higher dV/dt and dI/dt values than those of the S-MOS, indicating a better trade-off between switching loss and electromagnetic interference (EMI) noise.

Conclusion. A novel SiC SBD-wall-integrated trench MOSFET with semi-superjunction structure and STG is proposed. The figure of merit (FOM) of the S^3-TMOS is improved by 106% and 227% compared with that of S-MOS and C-TMOS, respectively. The STG, semi-superjunction, and P-Shield effectively reduce the coupling effect between gate and drain, and thus improve the switching characteristic. Wall-integrated SBD contributes to the decreasing of V_F. Compared to C-TMOS, the V_F and switching loss decreases by 42% and 70%, respectively. As a result, the S^3-TMOS achieves superior static and dynamic characteristics, indicating that the S^3-TMOS is competitive and promising in high power and high frequency application fields.

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