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Experimental investigation of the gate voltage range of negative differential capacitance in ferroelectric transistors

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Dear editor,

Recently, ferroelectric (FE)-based negative capacitance FET (NCFET) with ferroelectric/dielectric (FE/DE) gate stack has attracted extensive attention due to its capability of sub-60 mV/dec subthreshold swing (SS) at room temperature while maintaining a high on-state current compared with MOSFET [1]. However, the explanations of negative differential capacitance (NDC) in NCFET are still controversial. Different from the original quasi-static NC (QS-NC) theory, more research studies suggest that the transient NC is the reason for sub-60 SS in NCFET, and the NCFET performance can be influenced by the maximum range of sweeping gate voltage [2]. In our previous work, we have further experimentally clarified that the NDC phenomenon originates from the time-induced polarization increment of the ferroelectric film, and can only occur in a certain gate voltage range with strong sweeping rate dependence [3, 4]. The gate voltage range of NC effect emergence in this work refers to the corresponding applied voltage when FE voltage ($V_{\rm FE}$) is negative, rather than the maximum sweeping gate voltage. However, the physics of the certain gate voltage range is still not clear, and the impacts of sweeping rate and device parameters on the gate voltage range are also needed to be investigated.

In this work, the gate voltage range when the NC effect occurs is investigated in detail based on experimental results, and the influence of the applied sweeping rate ($\mathrm{d}V_{\rm G}/\mathrm{d}t$) and FE/DE capacitance matching are also demonstrated.

Experiments. In NCFET (Figure 1(a)), the SS of NCFET can be calculated by dividing the differential voltage amplification ($A_{\rm V}$) by the SS of MOSFET ($\mathrm{SS}_{\rm MOSFET}$), which can reflect the effect of amplification. When the differential FE voltage is negative ($\mathrm{d}V_{\rm FE}<0$), the $A_{\rm V}$ is larger than 1 and the SS of NCFET can be improved compared with $\mathrm{SS}_{\rm MOSFET}$. In this experiment, the NDC phenomenon in the NCFET gate stack is investigated by studying the ferroelectric voltage drop phenomenon in the FE/DE series capacitor as shown in Figure 1(b). The $\mathrm{Hf}_{0.5}\mathrm{Zr}_{0.5}\mathrm{O}_2$ film is deposited by the atomic layer deposition (ALD) with a Hf:Zr ratio of 0.5:0.5, after the annealing process at 500°C for 30 s, which shows the typical ferroelectric behavior verified by the X-ray diffraction (XRD) results (Figure 1(c)). As shown in the measured results in Figure 1(d), the NDC phenomenon occurs where $\mathrm{d}V_{\rm FE}$ is less than 0. Here, the beginning gate voltage and the sustained $V_{\rm G}$ of NDC phenomenon are defined as $V_{\rm NC\_begin}$ and $V_{\rm G\_range}$. The maximum $A_{\rm V}$ is defined as $A_{\rm V\_max}$.

Results and discussion. In ideal conditions the charge increments ($\mathrm{d}Q$) in the dielectric layers, the FE layer, and the channel are equal. For the FE/DE series structure, $\mathrm{d}V_{\rm G}=\mathrm{d}V_{\rm FE}+\mathrm{d}V_{\rm DE}$. Therefore, when the NC effect begins, the gate dielectric layer amplifies $\mathrm{d}V_{\rm G}$, which means $\mathrm{d}V_{\rm DE}$ caused by the $\mathrm{d}Q$ exceeds $\mathrm{d}V_{\rm G}$, as shown in the following formula:

$$\frac{\mathrm{d}Q}{\mathrm{d}t}=C_{\rm DE}\cdot\frac{\mathrm{d}V_{\rm DE}}{\mathrm{d}t}>C_{\rm DE}\cdot\frac{\mathrm{d}V_{\rm G}}{\mathrm{d}t}. \tag{1}$$

Therefore, it can be seen that the key of NC effect emergence is $\mathrm{d}Q/\mathrm{d}t$. The $\mathrm{d}Q$ comes from the polarization switching of FE. When further considering the different areas of the ferroelectric layer and dielectric layer, the equation can be rewritten as follows:

$$\frac{\mathrm{d}Q_0}{\mathrm{d}t}>\frac{\mathrm{d}V_{\rm G}}{\mathrm{d}t}\cdot\frac{\varepsilon_{\rm DE}\cdot S_{\rm DE}}{S_{\rm FE}\cdot d_{\rm DE}}, \tag{2}$$

$\mathrm{d}Q_0$ is the charge per area. It can be seen that the polarization charge required for the emergence of the NDC effect is determined by both the applied sweeping rate and the capacitance of FE/DE.

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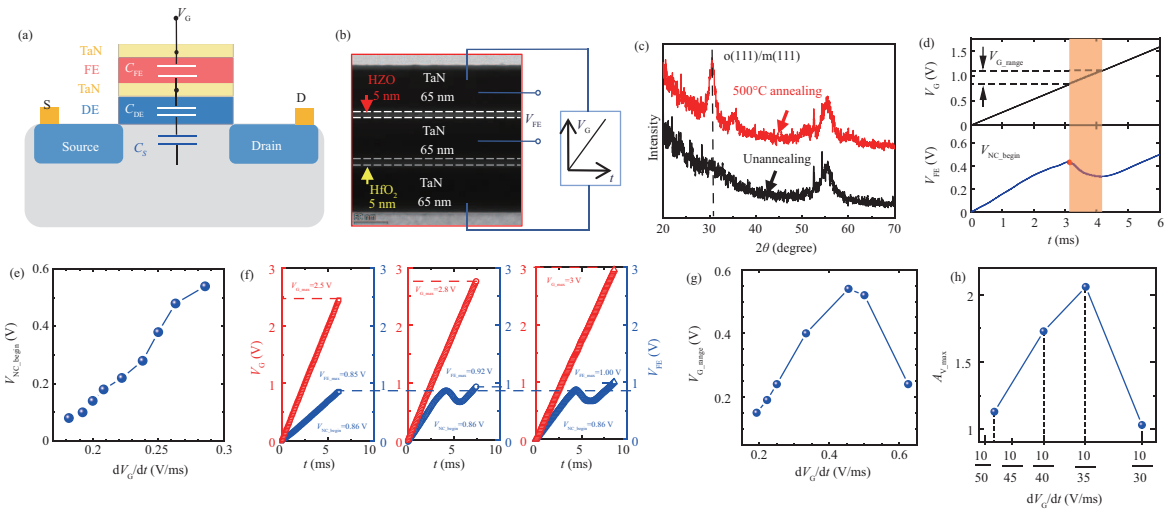

Figure 1 (Color online) (a) Schematic structure of NCFET; (b) cross-sectional TEM image of the FE/DE gate stack with schematic experimental setup for the measurement of V_{FE}-t; (c) the GI-XRD confirms the orthorhombic; (d) the input V_{G} and measured V_{FE} versus t; (e) measured $V_{\mathrm{NC\_begin}}$ versus applied sweeping rate; (f) measured V_{FE} versus t with different maximum V_{G} under the same sweeping rate of 2.5/7 (V/ms); (g) measured $V_{\mathrm{G\_range}}$ versus sweeping rate; (h) A_{V} versus $\mathrm{d}V_{\mathrm{G}}/\mathrm{d}t$ curves.

Based on the above analysis, the negative differential voltage behavior is strongly related to the switching rate. Figure 1(e) shows the measured and extracted $V_{\mathrm{NC\_begin}}$, which indicates that as the applied sweeping rate increases, the $V_{\mathrm{NC\_begin}}$ becomes larger. This is because according to (2), with the faster sweeping, the larger $\mathrm{d}Q/\mathrm{d}t$ is required for the NDC emergence, resulting in the larger $V_{\mathrm{NC\_begin}}$. Moreover, with a fixed sweeping rate, the V_{FE} decline behavior may not occur in NCFET when the required $V_{\mathrm{NC\_begin}}$ is too large and beyond the sweeping voltage range of V_{G}. As shown in Figure 1(f), with the same applied sweeping rate, the NDC effect may not occur when the ferroelectric partial voltage cannot reach $V_{\mathrm{NC\_begin}}$.

Moreover, with an increasing sweeping rate, the extracted $V_{\mathrm{G\_range}}$ and the $A_{\mathrm{V\_max}}$ will increase first and then decrease as shown in Figures 1(g) and (h). This is because the amount of charge increment for the emergence of NDC originates from the voltage-induced dielectric polarization and the time-induced ferroelectric polarization. When the NDC effect occurs, the V_{FE} starts to decrease with time increasing, the time-induced effect will keep promoting the polarization switching, while the voltage-induced effect is the opposite. Besides, as the applied sweeping rate increases, the $V_{\mathrm{NC\_begin}}$ becomes larger, and the more the polarized charge of the ferroelectric polarization can be accumulated with time. Therefore, the $A_{\mathrm{V\_max}}$ and $V_{\mathrm{G\_range}}$ will become larger with an increased sweeping rate. However, when the applied sweeping rate continues to increase, the required $\mathrm{d}Q/\mathrm{d}t$ also increases. It is more difficult to meet the requirements for the NDC emergence, resulting in the reduced $A_{\mathrm{V\_max}}$ and $V_{\mathrm{G\_range}}$, which is not beneficial for the device subthreshold swing.

Besides, the FE/DE capacitance may also impose requirements on the amount of $\mathrm{d}Q/\mathrm{d}t$ for the emergence of the NDC phenomenon. From Eq. (2), it can be seen that for a fixed ferroelectric capacitor, the larger dielectric capacitance results in the larger required $\mathrm{d}Q/\mathrm{d}t$ for NDC effect, and the corresponding V_{FE} ($V_{\mathrm{NC\_begin}}$) will also be larger.

With the FE/DE area ratio ($S_{\mathrm{FE}}/S_{\mathrm{DE}}$) increasing, the $V_{\mathrm{NC\_begin}}$ will decrease, which is because the larger $S_{\mathrm{FE}}/S_{\mathrm{DE}}$ requires less $\mathrm{d}Q/\mathrm{d}t$ per unit area. Besides, the smaller dielectric constant or the larger dielectric thickness will be similar to the situation of the larger $S_{\mathrm{FE}}/S_{\mathrm{DE}}$. For a practical device of NCFET, $S_{\mathrm{FE}}/S_{\mathrm{DE}}$ is always 1. To further reduce the $V_{\mathrm{NC\_begin}}$, the smaller dielectric constant or the larger dielectric thickness is required, which makes it a big challenge for the NCFET scaling. Although the current NCFET is not suitable for high-frequency low-voltage logic applications, the ferroelectric transistor can be used as a memory device, such as embedded non-volatile memory (NVM) applications and spiking neurons [5].

Conclusion. In this study, the impacts of sweeping rate and device parameters on the gate voltage range of the NDC phenomenon are investigated based on experiments. With the increase of the frequency and dielectric capacitance, the beginning gate voltage of the NC emergence will increase, and the gate duration voltage range and the maximum gate voltage amplification factor appear to increase first and then decrease. This work suggests a big challenge for scaled NCFETs to operate at high frequency with low V_{DD}.

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References

1 Salahuddin S, Datta S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. Nano Lett, 2008, 8: 405–410
2 Zhou J R, Wu J B, Han G Q, et al. Frequency dependence of performance in Ge negative capacitance pFETs achieving sub-30 mV/decade swing and 110 mV hysteresis at MHz. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2017. 373–376
3 Wang H M, Yang M X, Huang Q Q, et al. New insights into the physical origin of negative capacitance and hysteresis in NCFETs. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2018. 707–711
4 Wang H M, Huang Q Q, Yang M X, et al. Deep insight into the voltage amplification effect from ferroelectric negative capacitance. Sci China Inf Sci, 2019, 62: 089401
5 Chen C, Yang M, Liu S, et al. Bio-inspired neurons based on novel leaky-FeFET with ultra-low hardware cost and advanced functionality for all-ferroelectric neural network. In: Proceedings of Symposium on VLSI Technology (VLSI), 2019. 136–137