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Physical investigation of subthreshold swing degradation behavior in negative capacitance FET

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Abstract Power consumption has become one of the bottlenecks limiting the future development of integrated circuits. Tunnel FETs (TFETs) and negative capacitance FETs (NCFETs) can break the subthreshold swing limitation (60 mV/dec at room temperature) of conventional metal-oxide-semiconductor field-effect transistor (MOSFET) to reduce the operating voltage and thus power consumption. However, induced by the band-to-band tunneling mechanism, TFETs have a subthreshold swing degradation issue and relatively low ON current. Although NCFETs with ferroelectric/dielectric gate stack can theoretically maintain a high ON current comparable to conventional MOSFET, the physical origin of sub-60 SS is controversial and the mechanism of switching behavior in NCFET is still not clear. In this work, by experimentally investigating the whole negative differential capacitance process and its gate voltage amplification coefficient, an intrinsic issue of SS degradation with increased gate voltage is also found in NCFET for the first time. Based on the physical investigation and simulation results, it is shown that the intrinsic SS degradation in NCFET is resulting from the instant dielectric polarization response. Both the decrease of dielectric thickness and the increase of dielectric constant may lead to the severer SS degradation, which is not favorable for scaled NCFETs.

Keywords ferroelectric, negative differential capacitance effect, polarization, low power, voltage amplification

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1 Introduction

Power consumption has become the fundamental issue for nanoelectronic circuits. To reduce the operation voltage ($V_{\rm DD}$) for low power consumption while maintaining a high ON current, the device subthreshold swing (SS) needs to be reduced [1, 2], while traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) have a fundamental SS limitation of 60 mV/dec at room temperature. Tunnel FET (TFET) with band-to-band tunneling mechanism and negative capacitance FET (NCFET) with ferroelectric/dielectric (FE/DE) gate stack have attracted great attention due to their capability of sub-60 mV/dec SS at room temperature [3, 4]. However, for TFET, the ON current is relatively low, limiting its high-performance applications. Besides, the SS will increase with the increased gate voltage which is known as the SS degradation issue [5, 6]. The SS degradation issue may lead to the increase of average sub-threshold swing ($\rm SS_{avg}$) and thus $V_{\rm DD}$, which is not conducive to low consumption applications [7, 8].

Theoretically, NCFETs can maintain the high ON current comparable to conventional MOSFET [9–11]. Moreover, the NC effect of FE/DE gate stack in NCFET can achieve sub-60 mV/dec SS [12]. Concretely, the NC effect occurs when the reciprocal of the second derivation of potential energy (U) with respect to the ferroelectric polarization charge (Q) is negative [13], which means the differential capacitance ($\rm d$$Q$/$\rm d$$V$) is negative [14]. However, the theoretical explanation of negative differential capacitance is still

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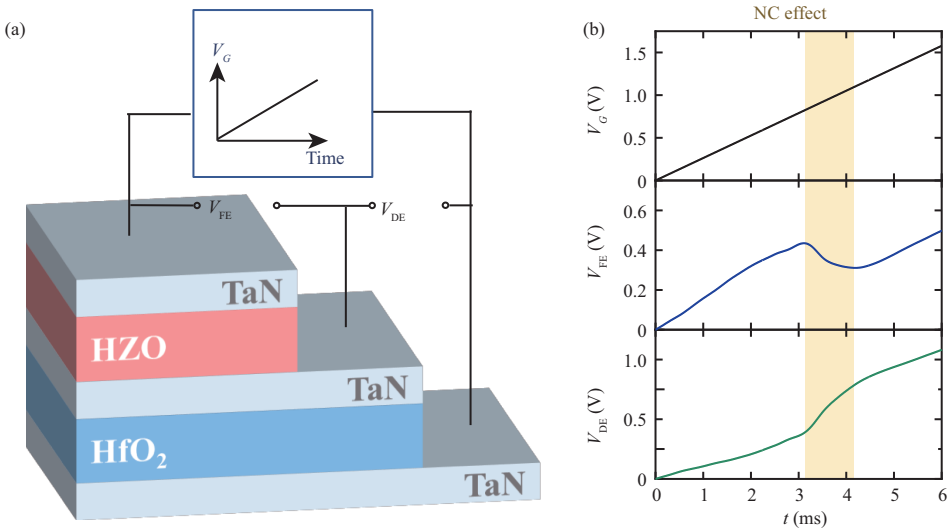

Figure 1 (Color online) (a) FE-DE series is a schematic representation of the NCFET gate stack. Measured $V_{\rm FE}$ and $V_{\rm DE}$ versus time in FE-DE series structure under constant applied voltage sweeping rate. (b) The input V_G versus t, and measured $V_{\rm FE}$ and $V_{\rm DE}$ versus t.

controversial and lacks direct experimental evidence. Currently, the main explanations for the sub-60 SS in NCFETs are the quasi-static NC (QSNC) and transient NC theory [15,16]. Based on the standalone ferroelectric capacitor, we have directly experimentally proved that the sub-60 SS of NCFET is originated from the dynamic polarization switching [17,18]. However, the electrical behavior and its inherent physics of SS with increased gate voltage in NCFET are still not clear.

In this paper, by experimentally investigating and analyzing the gate voltage amplification coefficient during the whole negative differential capacitance process, for the first time, it is found that the amplification coefficient shows non-monotonic dependence on gate voltage and there is an intrinsic issue of SS degradation with increased gate voltage in NCFET. It is shown that the physical origin of the SS degradation in NCFET is the dielectric polarization rather than the ferroelectric polarization. Both dielectric thickness decrease and the dielectric constant increase will lead to the severer SS degradation issue, which is not favorable for the scaled NCFETs.

2 Characterization of the gate voltage amplification in FE-DE series capacitance

The gate voltage amplification coefficient in NCFET, defined as A_V, can be obtained by using the internal gate voltage ($V_{\rm int}$) to divide the total applied voltage (V_G). The behavior of A_V can reflect the behavior of SS. A large A_V means a small SS in NCFET. To study the gate voltage amplification coefficient and the corresponding SS in NCFET, the gate stack in NCFET can be characterized by a series capacitance structure of ferroelectric and dielectric layers, as shown in Figure 1(a). The FE layer is a 5 nm $Hf_{0.5}Zr_{0.5}O_2$ film after the annealing process at 500°C for 30 s, which shows the typical ferroelectric polarization-voltage (P-V) loop behavior. The DE layer is a 5 nm HfO_2 film, whose capacitance is 8.3 μF/cm^2. The experimental details and the ferroelectric properties of HZO materials have been described in our previous work in detail [17,18].

Sweeping voltage signals with the constant rate are applied to the fabricated FE-DE series structure in this experiment, and the variable partial voltage of the ferroelectric layer and the dielectric layer in real-time responding to this external linear sweeping voltage (V_G-t) is monitored by an oscilloscope. As shown in the measured results in Figure 1(b), when the FE voltage ($V_{\rm FE}$) starts to decrease with the increased time, DE voltage ($V_{\rm DE}$) will increase more rapidly and thus the $V_{\rm DE}$-t curve becomes steeper with a larger change rate, and the change rate of $V_{\rm DE}$ becomes to exceed the sweeping rate of external applied voltage, which also means the differential voltage of the DE layer is amplified and A_V>1 can be achieved.

According to $V_{\rm FE}$ and $V_{\rm DE}$, the gate voltage amplification coefficient A_V and the charge change over time dQ/dt can be extracted. In this work, A_V is experimentally extracted by using d$V_{\rm FE}$/dt and dV_G/dt

and satisfies the following equation:

$$A_V = \frac{\mathrm{d}V_{\mathrm{int}}}{\mathrm{d}V_G} = -\frac{\mathrm{d}V_{\mathrm{FE}}/\mathrm{d}t}{\mathrm{d}V_G/\mathrm{d}t}. \tag{1}$$

Considering the fixed capacitance of the DE layer (C_{DE}), the charge change on the electrode satisfies the following equation, which means that $\mathrm{d}Q/\mathrm{d}t$ can be obtained by the measured $\mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t$:

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = C_{\mathrm{DE}} \times \mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t. \tag{2}$$

3 Results and discussion

3.1 Dynamic polarization charge in ferroelectric HfO_2

For the FE-DE series stack, when the NC effect occurs, the dielectric voltage increment ($\mathrm{d}V_{\mathrm{DE}}$) will exceed the total gate voltage increment ($\mathrm{d}V_G$), which is originated from the change of dynamic polarization charge increment ($\mathrm{d}Q$). The requirement of $\mathrm{d}Q$ for the negative differential capacitance effect is shown in the following equation:

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = C_{\mathrm{DE}} \times \mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t > C_{\mathrm{DE}} \times \mathrm{d}V_G/\mathrm{d}t. \tag{3}$$

Therefore, it can be seen that the key of NC effect emergence is $\mathrm{d}Q$, which comes from the dynamic polarization switching. In the FE layer, the dynamic polarization charge Q consists of ferroelectric polarization and dielectric polarization, where ferroelectric polarization will increase with time and voltage, and dielectric polarization has a positive dependence on voltage, as shown in the following equation [19]:

$$Q = \varepsilon_0 E + P = (1+\chi)\varepsilon_0 E + P_{\mathrm{re}} = P_t + P_{\mathrm{re}}, \tag{4}$$

where χ is polarizability, ε_0 is vacuum dielectric constant, E is the electric field, P_{re} is ferroelectric spontaneous polarization, and P_t is dielectric polarization. With the increased voltage changing, the dielectric polarization switching can respond instantaneously, while the ferroelectric polarization switching also depends on time. Therefore, to study the physical process of the NC effect in ferroelectric materials, both ferroelectric and dielectric polarization should be considered, especially for multi-phase ferroelectric HfO_2 material [20]. Grown by the ALD process, the ferroelectric HZO material is mostly multi-phase, and both relaxation-responsive ferroelectric phase and instant-responsive dielectric phase exist [9].

3.2 Gate voltage amplification and SS degradation

Figure 2 shows the experimentally extracted A_V and $\mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t$ of our fabricated FE-DE series structure. When the FE-DE series structure is applied to constant sweeping rate voltage, the partial voltage of the FE layer and DE layer changes with external applied voltage nonlinearly, resulting from the ferroelectric polarization. As shown in Figure 2(a), the red solid curve represents the change of FE layer amplification coefficient A_V with time, and the blue dotted curve corresponds to the V_{FE}-t. Under a certain sweeping rate, the FE layer can be in the NC state, and thus negative $\mathrm{d}V_{\mathrm{FE}}$ and $A_V > 1$ can be observed. Figure 2(b) shows the observed $\mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t$ when positive $\mathrm{d}V_G/\mathrm{d}t$ is applied and negative $\mathrm{d}V_{\mathrm{FE}}$ occurs.

Since V_G increases linearly with time, these experimental A_V-t results can also reflect the behavior of A_V with increased gate voltage. During the NC effect, with increased V_G, A_V increases at first and then decreases, which indicates that the SS of NCFET is not a constant as the gate voltage increases. Instead, for NCFET, the device SS may reduce at first and then inevitably increase. The measured negative capacitance characteristics with the non-monotonic gate voltage amplification phenomenon in this work have been found in dozens of our fabricated devices, which indicates that the results are reliable and reproducible.

For a logic device, to reduce the operating voltage and the power, it requires not only steep minimum SS ($\mathrm{SS_{min}}$) but also steep average SS ($\mathrm{SS_{avg}}$, usually defined as the average SS extracted from off state to threshold state) [21] to ensure a high on-off current ratio ($I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio). The increasing SS with the increasing gate voltage, called the SS degradation behavior in this work, will increase $\mathrm{SS_{avg}}$, which is not conducive to improve $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and reduce V_{DD} [22]. Unfortunately, it is found that NCFET has the inherent SS degradation issue like TFET, although their physical mechanisms are different.

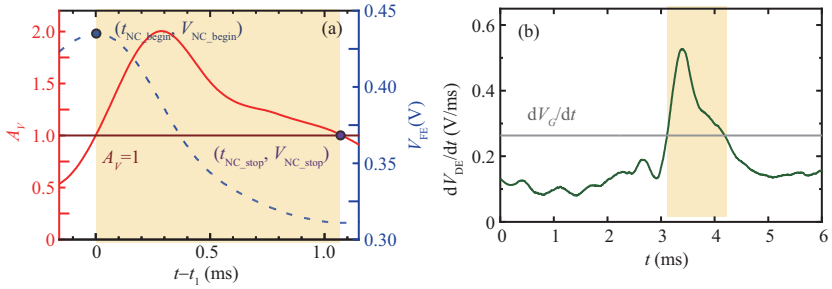

Figure 2 (Color online) (a) According to the relationship between voltage and electrical charges, the amplification factor $A_V = 1 - \mathrm{d}V_{\mathrm{FE}}/\mathrm{d}V_G$ in the experiment is extracted and plotted in a red solid line, based on the measured voltage shown in a blue dotted line. The time and voltage at the point where V_{FE} starts decreasing are defined as $t_{\mathrm{FE\_begin}}$ and $V_{\mathrm{FE\_begin}}$. (b) During the NC effect stage, $\mathrm{d}V_{\mathrm{DE}}/\mathrm{d}t$ exceeds $\mathrm{d}V_G/\mathrm{d}t$.

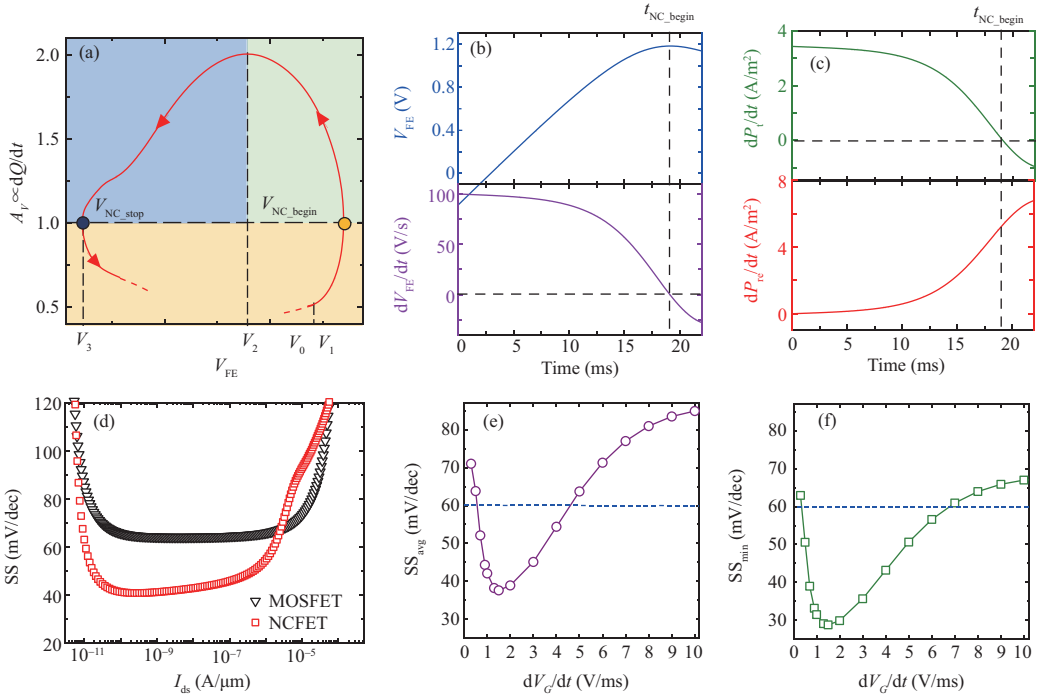

Figure 3 (Color online) (a) Extracted A_V is as a function of V_{FE}. A_V is proportional to $\mathrm{d}Q/\mathrm{d}t$. NC effect starts at $V_{\mathrm{NC\_begin}}$. NC effect stops at $V_{\mathrm{NC\_stop}}$. (b) Simulated V_{FE} and $\mathrm{d}V_{\mathrm{FE}}/\mathrm{d}t$ by TCAD. (c) Simulated $\mathrm{d}P_t/\mathrm{d}t$ and $\mathrm{d}P_{\mathrm{re}}/\mathrm{d}t$ by TCAD. During NC effect, $\mathrm{d}P_t/\mathrm{d}t$ is negative and $\mathrm{d}P_{\mathrm{re}}/\mathrm{d}t$ is positive. (d) Simulated SS behaviors in NCFET and MOSFET. (e) Extracted simulated $\mathrm{SS}_{\mathrm{avg}}$ of NCFET with different sweeping rates. (f) Extracted simulated $\mathrm{SS}_{\mathrm{min}}$ of NCFET with different sweeping rates.

3.3 Physical mechanism of SS degradation in NCFET

To investigate the physical mechanism of SS degradation in NCFET, we convert the measured curve of A_V versus time in Figure 2(a) into the curve of A_V versus V_{FE} in Figure 3(a), where A_V is proportional to charge increment $\mathrm{d}Q/\mathrm{d}t$. The ferroelectric voltage corresponding to the beginning of the NC effect is defined as $V_{\mathrm{NC\_begin}}$. The FE voltage corresponding to the ending of the NC effect is defined as $V_{\mathrm{NC\_stop}}$. We note that the ferroelectric voltage during the whole NC effect process keeps decreasing. In this process, $\mathrm{d}Q/\mathrm{d}t$ is increasing at first and then decreasing, which is the same as A_V in Figure 2(a).

To explain the experimental phenomena above, the polarization switching behavior during the whole NC process is analyzed and simulated considering both instant-responsive dielectric polarization and relaxation-responsive ferroelectric polarization based on the Sentaurus TCAD tools. In Sentaurus TCAD, both FE-DE series capacitor and NCFETs are simulated considering 2-D Poisson's equation and carrier continuity equations self-consistently [23]. More details of simulation methods have been described in our previous work [18].

Figures 3(b) and (c) show the simulation results of the FE-DE series capacitor, and both ferroelectric

spontaneous polarization and dielectric polarization are respectively simulated and extracted. It can be seen that the change direction of $\mathrm{d}P_t/\mathrm{d}t$ is always consistent with the direction of electric field change ($\mathrm{d}E/\mathrm{d}t$), while the $\mathrm{d}P_{\mathrm{re}}/\mathrm{d}t$ is simultaneously affected by voltage and time change.

As shown in Figure 3(a), before NC effect begins, $\mathrm{d}Q/\mathrm{d}t$ is increasing when ferroelectric voltage increases, which consists of ferroelectric response and dielectric response, and can be written in the following formula:

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = \frac{(1+\chi)\varepsilon_0}{d} \cdot \frac{\mathrm{d}V_{\mathrm{FE}}}{\mathrm{d}t} + \frac{\mathrm{d}P_{\mathrm{re}}}{\mathrm{d}t}. \tag{5}$$

Therefore, from Figure 3(b), it is known that $\mathrm{d}V_{\mathrm{FE}}/\mathrm{d}t$ will decrease before NC effect begins, which means $\mathrm{d}P_t/\mathrm{d}t$ will decrease, while $\mathrm{d}P_{\mathrm{re}}/\mathrm{d}t$ keeps increasing with increasing applied voltage NC. According to the derivation of our previous work [18], with $\mathrm{d}Q/\mathrm{d}t$ increasing, when $\mathrm{d}V_{\mathrm{DE}}$ increases to exceed $\mathrm{d}V_G$, A_V will exceed 1 and ferroelectric voltage begins to drop, corresponding to the appearance of NC phenomenon.

When the negative differential capacitance phenomenon occurs, according to the measured results, it can be seen that $\mathrm{d}Q/\mathrm{d}t$ first increases and then decreases. This is because as the ferroelectric voltage decreases, the instant-responsive dielectric polarization P_t decreases and $\mathrm{d}P_t$ becomes negative, hindering the increase of $\mathrm{d}Q/\mathrm{d}t$ for gate voltage amplification. However, at this time, the increasing ferroelectric polarization P_{re} is still promoting the gate voltage amplification for larger A_V. Therefore, there is a competition between the effects of these two polarizations. At the beginning stage when $A_V > 1$, the role of P_{re} dominates and thus the gate voltage amplification coefficient increases with the gate voltage or time. However, as the time continues to increase, the gate voltage amplification coefficient increases rapidly, leading to a rapid decrease of the ferroelectric voltage and a more significant hinder effect induced by P_t. Therefore, when the role of dielectric polarization P_t dominates and the gate voltage amplification coefficient starts to decrease, corresponding to the long-lasting SS degradation behavior in NCFET. Finally, the NC phenomenon will end when (3) cannot be satisfied.

From the above discussion, it can be seen that the dielectric polarization is the essential physical origin for the inevitable degradation of SS in NCFET. To further investigate the SS degradation behavior, NCFET devices are simulated based on Sentaurus TCAD tools, and the SS of NCFET and MOSFET is extracted and compared as shown in Figure 3(d), which also demonstrates the degradation behavior of SS in NCFET.

For NCFET, the sweeping rate can significantly impact the ferroelectric response and thus the NC effect [17]. Therefore, $\mathrm{SS_{avg}}$ will also change with different sweeping rates. As shown in the extracted simulation results in Figure 3(e), it is found that $\mathrm{SS_{avg}}$ will first decrease and then increase with the increasing sweeping rate. Compared with Figure 3(f), the frequency range of $\mathrm{SS_{avg}}$ below 60 mv/dec is more stringent than that of $\mathrm{SS_{min}}$ due to the influence of SS degradation. As shown in Figure 3(e), when the sweeping rate for NCFET is in the range of 5 to 7 V/ms, although $\mathrm{SS_{min}}$ is still below 60 mV/dec, $\mathrm{SS_{avg}}$ is more than 60 mV/dec due to the dominant effect of SS degradation. When the sweeping rate further increases, the $\mathrm{SS_{min}}$ is also larger than 60 mV/dec because the ferroelectric polarization switching cannot respond to the gate voltage sweeping.

According to (5), during the negative differential capacitance process, the decrease of dielectric thickness and the increase of dielectric constant will make the dielectric polarization more dominant, which may lead to a severer SS degradation issue. It is not favorable for the scaled NCFETs and puts forward new challenges for logic applications.

4 Conclusion

In this work, the physical process of NC effect is analyzed comprehensively from the perspective of ferroelectric polarization and dielectric polarization, and the intrinsic SS degradation issue in NCFET is found and explained. The phenomenon that the gate voltage amplification coefficient increases at first and then decreases is due to the competition effects between ferroelectric polarization and dielectric polarization. The role of ferroelectric polarization dominates at the beginning of the negative differential capacitance process, while with ferroelectric voltage continuing to reduce, the effect of dielectric polarization increases rapidly, leading to the essential SS degradation behavior with increased gate voltage in NCFET. Moreover, the decrease of dielectric thickness and the increase of dielectric constant will make SS degradation issue severer.

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