

IGZO-based neuromorphic transistors with temperature-dependent synaptic plasticity and spiking logics

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Abstract Temperature is one of the vital influential factors for all physiological and mental activities. Studying the influence of temperature on the properties of synaptic devices is of great importance for neuromorphic computing and bionic perception. Here, indium-gallium-zinc-oxide (IGZO) based electrical-double-layer neuromorphic transistors were proposed for the emulation of temperature-dependent synaptic functions. The influence of temperature on the synaptic plasticity, including excitatory postsynaptic current, paired-pulse facilitation, and dynamic filtering was investigated. Interestingly, temperature induced spiking AND to OR logic switching was demonstrated in an IGZO-based neuromorphic transistor with two in-plane gate electrodes. Our results provided an insight into the temperature-induced synaptic functions and spiking logic switching, which is interesting for neuromorphic systems with biological fidelity.

Keywords neuromorphic transistors, IGZO TFTs, temperature-dependent synaptic plasticity, logic transformation

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1 Introduction

Almost all life activities of organisms should stay within an appropriate temperature range, especially for warm-blooded animals represented by human beings. In neurology, a temperature is an influential factor of living cells, and it would affect virtually every aspect of the neuronal functions, including enzymatic activity, metabolism, ion channel kinetics, and synaptic transmission [1–4]. For example, the synaptic plasticity, interpreted by the modulation of synaptic strength or synaptic weight by the concentrations of ionic species (e.g., Ca^{2+} , Na^+ , K^+) [5–7], is highly sensitive to temperature. When the temperature is lower than normal temperature, the release of neurotransmitters and fluxes of ions would decrease, and the information process would be impeded [8, 9]. With the increase of temperature, the activity of ion channel and the rate of ion exchange would be enhanced [10]. However, when the temperature further increases, the ions would overload, and the structure of cells may be directly destroyed by the physical effect [11].

Neuromorphic electronics, aimed at translating neurological superiorities to electronics, is highly dependent on the fidelity level that can be achieved [12–15]. For example, a hardware neural network with the functional dendritic component and remarkable energy efficiency has been demonstrated recently [16]. As a fundamental sub-topic, the development of biologically plausible synaptic devices would underlie the pursuit of high fidelity at the system level. Hence, a broad spectrum of electronic devices that are implicit with synapse-like ion dynamics, have been proposed, and essential synaptic plasticity such as excitatory postsynaptic current (EPSC), paired-pulse facilitation (PPF), and dynamic filtering, have been well mimicked by them [17–20]. However, the short of neuromorphic devices that can imitate

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the temperature-induced synaptic function modulation and the poor understanding of these emulations would further hinder the development of neuromorphic systems with high biological fidelity. Recently, the temperature was used as a parameter to modulate the synaptic plasticity and accelerate the learning process of artificial synapses in some synaptic devices like floating gate transistors and memristive devices [21, 22]. By given this, further studies of the influence of temperature on synaptic devices are very important for neuromorphic computing and bionic perception.

Indium-gallium-zinc-oxide (IGZO) based electrical-double-layer (EDL) transistor is a promising platform to implement the temperature-induced synaptic function emulations due to the internal thermodynamic process of proton motion in the gate dielectric of the solid-state electrolyte [23–25] as well as the success in synaptic emulations [19, 26, 27]. In this work, temperature-dependent synaptic function emulation was realized in an IGZO-based neuromorphic transistor, demonstrating one-step toward biological fidelity in terms of temperature. Synaptic plasticity including EPSC, PPF, and dynamic filtering was mimicked. More interestingly, spiking AND logic to OR logic switching was demonstrated in an IGZO-based neuromorphic transistor with two in-plane gate electrodes. Our results provide a way of high biological fidelity emulation, and further enrich the construction of neuromorphic system.

2 Experimental

For neuromorphic transistor fabrication, solid-state electrolyte film of chitosan is used as the gate dielectric, and amorphous IGZO film is used as the channel layer, respectively. Firstly, the chitosan powder ($\geq 99.5\%$, Aldrich) was dissolved in deionized water and acetic acid solvent to form a 2 wt% chitosan solution, where the acetic acid was used to provide more mobile protons for the formation of EDL. The weight ratio of chitosan powder, acetic acid and deionized water is about 1:1:50. Then, chitosan electrolyte solution was coated onto an indium-tin-oxide (ITO)-glass substrate and the chitosan film was dried in the atmosphere for about one day to form an insulating layer with a thickness of around 10 μm . Thirdly, patterned IGZO thin films (size: 680 $\mu\text{m} \times 1300 \mu\text{m}$) were deposited on the chitosan electrolyte film by radio frequency magnetron sputtering with a metal shadow mask using an IGZO target (In:Ga:Zn = 2:2:1 atom ratio) at room temperature. During the sputtering, the Ar flow rate, the cavity pressure, and the sputtering power were 30 sccm, 0.45 Pa, and 100 W, respectively. The thickness of the IGZO thin film was about 40 nm. Lastly, patterned Ag source/drain electrodes and multiterminal in-plane gate electrodes with a thickness of about 80 nm were deposited by thermal evaporation with another metal shadow mask. The channel length/width is 80 $\mu\text{m}/1000 \mu\text{m}$, and the size of the Ag electrodes is 150 $\mu\text{m} \times 1000 \mu\text{m}$. Figure 1(b) shows a schematic structure of an IGZO-based neuromorphic transistor with chitosan electrolyte as gate dielectric. The metal-electrolyte-metal capacitor structure was directly thermal evaporated Ag electrode (size: 150 $\mu\text{m}/1000 \mu\text{m}$) onto the chitosan thin film with a metal shadow mask as shown in the inset of Figure 2(c). The capacitance of the chitosan film was measured by an impedance analyzer (HIOKI IM 35522-01 LCR meter). The electrical characteristics of the devices were measured by source measurement units (Keithley 2636B) at a relative humidity of 50%. Temperature changing is achieved by heating the devices on a heating plate.

3 Results and discussion

A biological synapse performs signal transmission and information processing among neurons by conducting electrically triggered fluxes of ionic species [20, 28]. A detailed schematic diagram of a chemical synapse with different temperatures is illustrated in Figure 1(a). When an action potential arrives in the pre-synapse, it triggers the release of neurotransmitters. The neurotransmitters diffuse to the post-synaptic membrane, leading to the flow of ions and changing the membrane conductance of postsynaptic neurons [29]. In this study, we fabricated an IGZO-based EDL neuromorphic transistor to emulate the temperature-dependent synaptic functions, as shown in Figure 1(b). In this synaptic transistor, voltage pulses applied on the bottom and lateral gate electrodes are considered as the presynaptic spikes, and the current in the channel is regarded as the postsynaptic activity, respectively. The mobile protons in the chitosan dielectric layer act as neurotransmitters and migrate in response to presynaptic spikes. The detailed fabrication processes of the IGZO-based EDL synaptic transistor are described in Section 2. Figure 1(c) shows the equivalent electrical circuit diagram of the synaptic transistor.

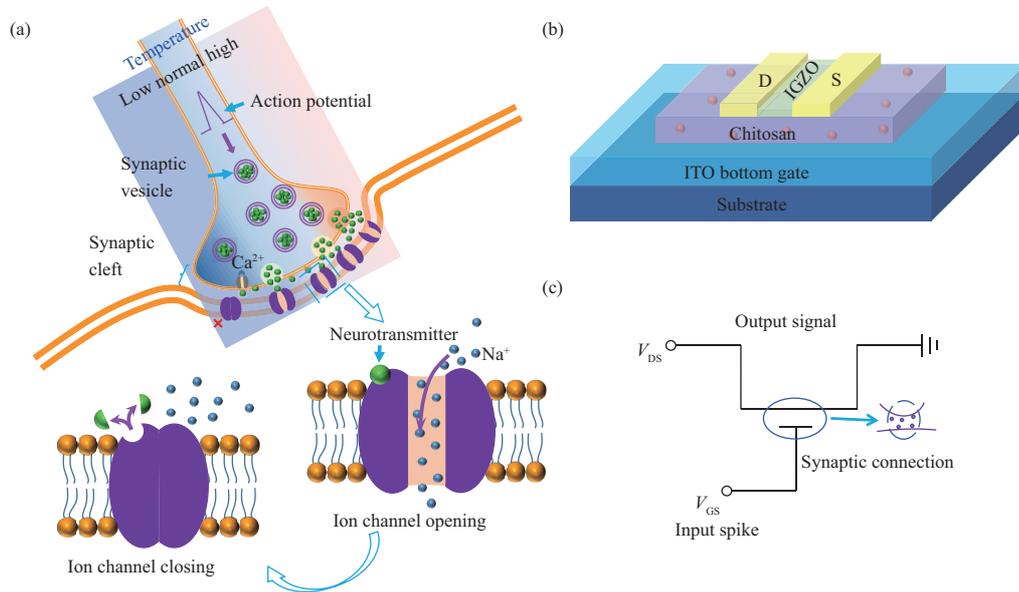


Figure 1 (Color online) Structure diagrams of the biological synapse and the neuromorphic transistor. (a) A detailed schematic illustration of a chemical synapse under different temperatures with information transmission; (b) a schematic diagram of an IGZO-based EDL synaptic transistor; (c) the equivalent electrical circuit of the synaptic transistor.

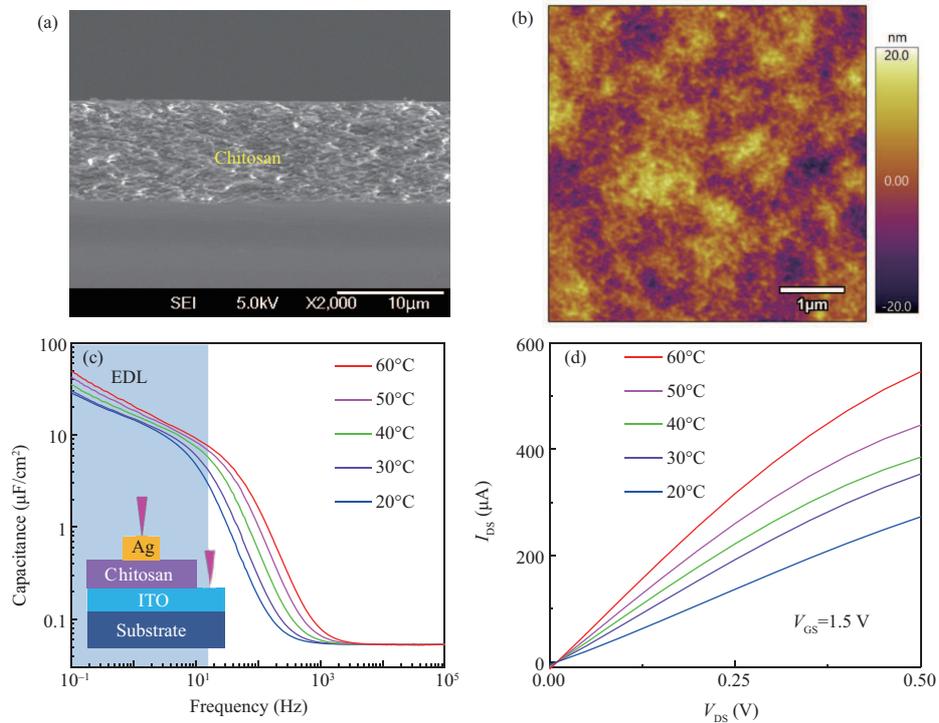


Figure 2 (Color online) Characterization of the neuromorphic transistor. (a) Cross-sectional SEM image of a chitosan electrolyte membrane on a Si (100) substrate; (b) AFM image of the surface morphology of the chitosan dielectric membrane on a Si (100) substrate; (c) frequency-dependent specific capacitance curves of the chitosan electrolyte film measured at different temperatures, inset: a schematic diagram of the Ag/chitosan electrolyte membrane/ITO sandwich structure; (d) the output current-voltage characteristics of the IGZO-based EDL synaptic transistor with V_{GS} of 1.5 V at different temperatures.

The gate dielectric of this neuromorphic transistor is chitosan electrolyte, which has a large EDL capacitance at low frequency. Figure 2(a) shows a cross-sectional scanning electron microscopy (SEM) image of the chitosan electrolyte film on a Si (100) substrate, and the thickness of the chitosan film is

estimated to be $\sim 10 \mu\text{m}$. Figure 2(b) shows an atomic force microscope (AFM) image of the surface topography of the chitosan film on a Si (100) substrate. The root-mean square (RMS) roughness of the chitosan film surface is estimated to be $\sim 3.0 \text{ nm}$. Frequency-dependent capacitance characteristics of the chitosan electrolyte film were measured in a vertical Ag/chitosan electrolyte/ITO sandwich structure (inset of Figure 2(c)). As shown in Figure 2(c), a large EDL capacitance $> 1.0 \mu\text{F}/\text{cm}^2$ at 20°C , 30°C , 40°C , 50°C , and 60°C can be obtained when the frequency is lower than 10 Hz. When the temperature increases, the specific capacitance values also increase at each frequency. Accumulation of protons at the interface of chitosan electrolyte/ITO electrode can result in a large EDL capacitance, and the increase of temperature will accelerate the movement of protons in the chitosan film, which contributes to the increase of the capacitance. Figure 2(d) shows the output curves of the IGZO-based EDL neuromorphic transistor at different temperatures. When the temperature increases from 20°C to 60°C , the output current (I_{DS}) measured at $V_{\text{DS}} = 0.5 \text{ V}$ increases from ~ 273.1 to $\sim 545.9 \mu\text{A}$. The temperature has an obvious influence on the mobility, threshold voltage, and subthreshold swing, which have been investigated [30–32]. When the temperature increases, protons in the chitosan film will move faster and more protons will accumulate on the channel/dielectric interface, which will induce more electrons in the IGZO channel layer.

EPSC can be triggered by a presynaptic spike and can temporally last for $\sim 1\text{--}10^4 \text{ ms}$ [33,34]. In order to measure the temperature-dependent EPSC of the IGZO-based transistor, we applied a presynaptic spike (1.0 V, 25 ms) to the gate electrode and measured the postsynaptic current with a constant drain-source voltage (V_{DS}) of 0.5 V at different temperatures. Figure 3(a) shows the presynaptic potentials (1.0 V, 25 ms), and the EPSCs triggered by the presynaptic spike at different temperatures, respectively. The amplitudes of the EPSCs at 20°C , 30°C , 40°C , 50°C and 60°C are about 6.2, 12.8, 29.1, 187.7, and 549.9 nA, respectively. Figure 3(b) shows the conductance (G) as a function of negative reciprocal of temperature ($-1000/T$). The G is derived by $G = I/U$, where I and U are the peak of EPSC and the measuring voltage between source and drain electrodes, respectively. The relationship between conductance and temperature follows a formula: $G \propto \exp(-E/kT)$, where E is the activation energy, and k is the Boltzmann's constant [35,36]. The biomimetic electrical behavior originates from proton migration in the chitosan dielectric layer. When a presynaptic spike (1.0 V, 25 ms) was applied to the bottom gate electrode, the protons were driven to move toward the interface of chitosan layer/IGZO channel, resulting in the accumulation of electrons on the interface of IGZO channel/chitosan dielectric layer, which induced the increase of postsynaptic current at the drain electrode. The detailed process is shown in Figure 3(c). After the presynaptic spike was removed, the protons gradually drifted back to random equilibrium positions in the chitosan layer, as shown in Figure 3(d). The movement of ions with different temperatures is also demonstrated in Figure 3(c) and (d). The length of the arrow line represents the speed of the ion movement. When the temperature increases, the protons will move faster, which results in the increase of the EPSCs.

To further study the temperature-dependent synaptic functions, PPF was also demonstrated in this work. In a biological neural system, PPF is a behavior of short-term synaptic plasticity, and is considered to be associated with short-term adaptation to sensory inputs and short-lasting form of memory [6,37]. PPF is triggered by a pair of stimuli, and the amplitude of the EPSC triggered by the second spike (A_2) can be several times of the EPSC triggered by the first one (A_1). Figure 4(a) shows the PPF behaviors mimicked in the IGZO-based EDL synaptic transistor at 20°C , 40°C and 60°C , respectively. The PPFs were triggered by a pair of presynaptic spikes (1.0 V, 25 ms) with a time interval of 25 ms between the pair of stimuli. The amplitude of the PPF triggered by the second spike is about 1.06, 1.86, and 1.28 times of that triggered by the first one at 20°C , 40°C and 60°C , respectively. Figure 4(b) shows the ratio of A_2/A_1 as a function of time interval (Δt) at different temperatures, and it is well fitted by a double-exponential decay function [5]:

$$\text{PPF ratio} = 1 + C_1 \exp(-\Delta t/\tau_1) + C_2 \exp(-\Delta t/\tau_2), \quad (1)$$

where C_1 and C_2 are the initial facilitation magnitudes of the rapid and slow phases, respectively. τ_1 and τ_2 are the characteristic relaxation times of the rapid and slow phases, respectively. Δt is the interval time between a pair of triggered spikes.

The amplitude of the PPF ratio decreases with the increase of Δt . When the time interval between the pair of stimuli is shorter than the relaxation time of the protons in the chitosan electrolyte, some of the protons triggered by the first spike cannot diffuse back to their equilibrium position before the second spike arrives. It can be observed from Figure 4(a) that the amplitude of the PPF ratio at 40°C is larger than that at 20°C and 60°C which may be due to the proton moving too slowly at low temperature

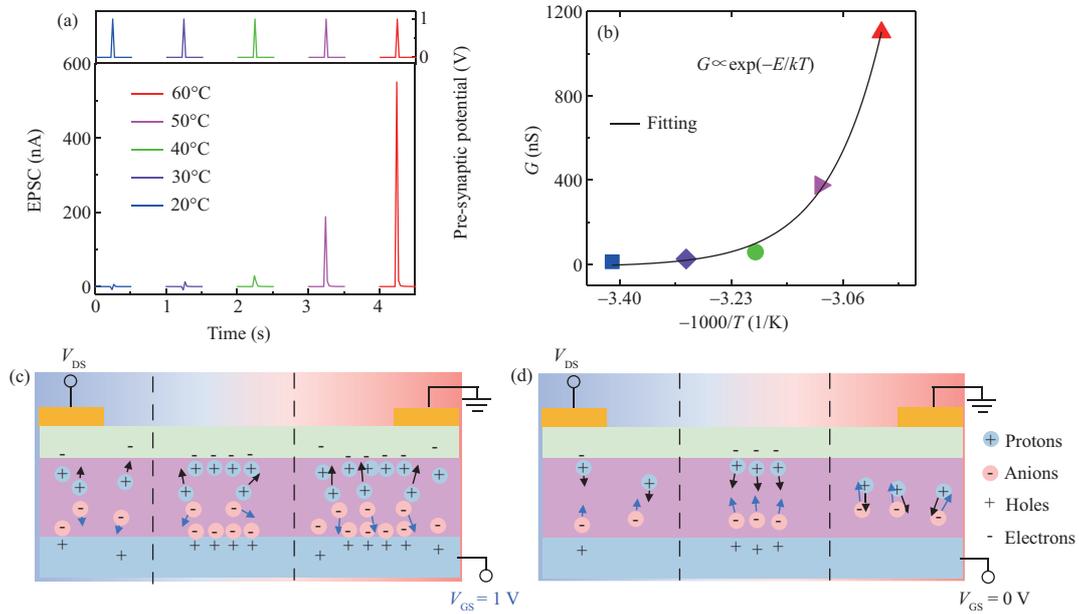


Figure 3 (Color online) Modulatory synaptic plasticity of EPSCs at different temperatures. (a) Presynaptic spikes (1.0 V, 25 ms) and the EPSCs triggered by presynaptic potential at different temperatures, respectively; (b) G as a function of $-1000/T$. Cross-section view of the neuromorphic transistor with the gate voltage (c) applied and (d) removed at low, normal, and high temperature. The gate voltage is 1.0 V, and the length of the arrow line represents the speed of the ions' movement.

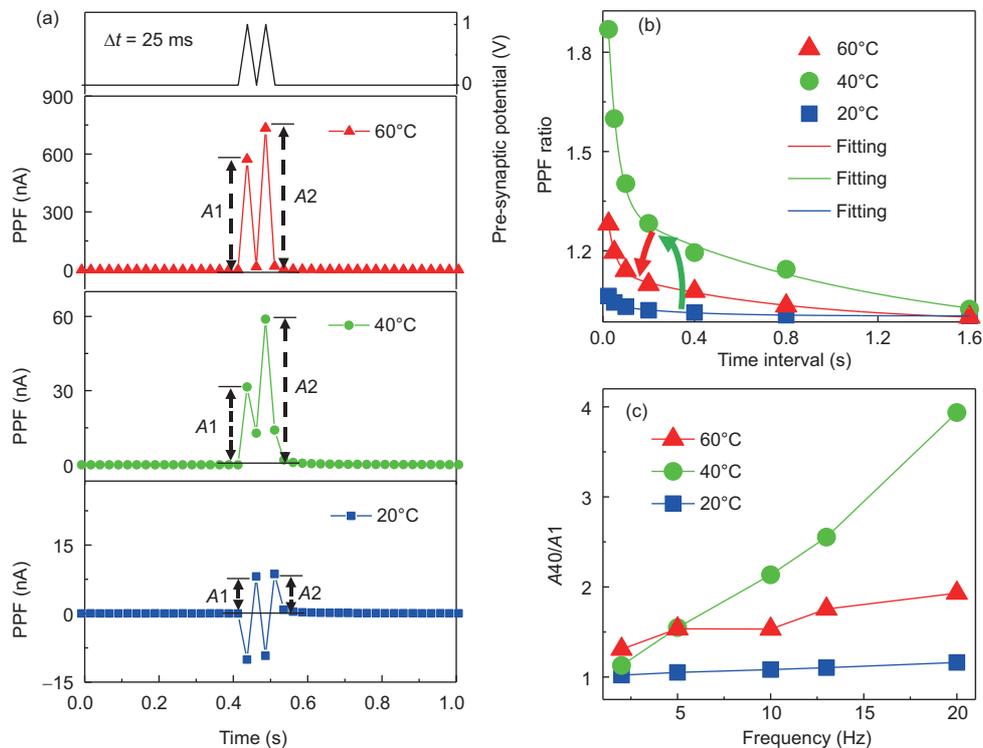


Figure 4 (Color online) PPF and high pass filter characteristics. (a) The postsynaptic current triggered by a pair of presynaptic spikes (1.0 V, 25 ms) applied to the gate electrode as a function of time at different temperatures; (b) the PPF ratio as a function of the time interval between the pair of presynaptic spikes with different temperatures; (c) the gain of A_{40}/A_1 as a function of frequency with different temperatures.

and too fast at high temperature. Just as shown in Figure 3(c) and (d), when the temperature is 20°C and the first spike is applied on the gate electrode, few protons are accumulated at the interface of the chitosan electrolyte/IGZO channel. Afterwards, when the second spike arrives, still very few protons move to the interface of chitosan electrolyte/IGZO channel. Therefore, the gain of PPF is small at 20°C

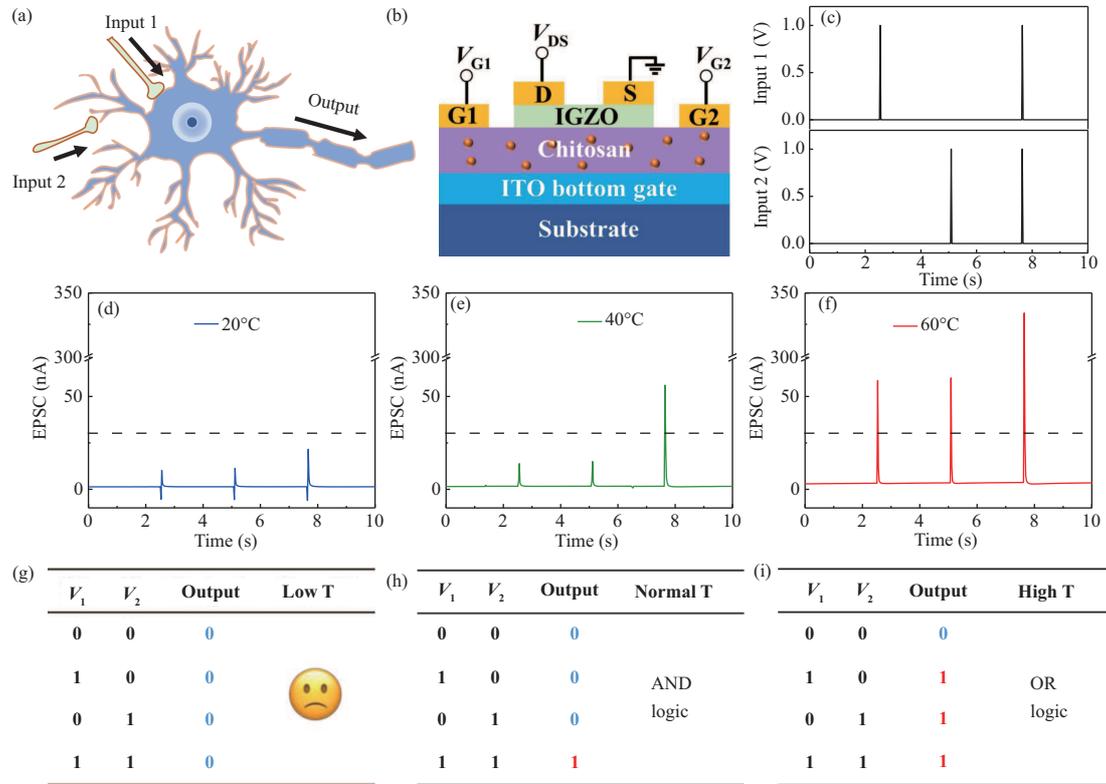


Figure 5 (Color online) Multiterminal neuromorphic transistor and logic functions. (a) A schematic illustration of a neuron with two synaptic inputs and one output; (b) the schematic diagram of a multiterminal in-plane lateral coupled synaptic transistor for logic signal processing; (c) two presynaptic input pulse trains (1.0 V, 25 ms); (d)–(f) the output current triggered by the presynaptic pulses at 20°C, 40°C, and 60°C, respectively; (g)–(i) the truth tables at 20°C, 40°C, and 60°C, respectively.

When the temperature is 60°C and the first spike is applied on the gate electrode, although a large number of protons accumulate at the interface of the chitosan electrolyte/IGZO channel, they would quickly diffuse back to their equilibrium position when the first spike is removed. Then, when the second spike arrives, the protons repeat this movement. So, a small amount of protons accumulated on the interface of chitosan/IGZO channel, and the gain of PPF is also very small. From these results, when the temperature is too low or too high, the PPF characteristic obviously shows a small gain, which is similar to the behavior of our neural system.

Short-term plasticity underlies temporal filtering by impeding or facilitating synaptic transmission [38]. High-pass filtering is an important temporal filtering function of synapses. Since a higher PPF gain could be obtained with a shorter time interval, high-pass filtering can also be achieved in such neuromorphic transistors [17, 39]. In order to emulate the high-pass filtering function of a synapse, spike trains with different frequencies were applied onto the gate electrode of the synaptic transistor at different temperatures. The pulse trains of each frequency are composed of 40 spikes (1.0 V, 25 ms). Figure 4(c) shows the frequency-dependent gain defined by the ratio of the EPSC peak of the fortieth (A_{40}) and the first (A_1) at different temperatures. The highest high-pass filtering gain (A_{40}/A_1) is realized when the temperature is 40°C as shown in Figure 4(c). As a result, the gain can be modulated by the temperature applied onto the device. This performance is consistent with the PPF characteristics with the temperatures, and the temperature-dependent synaptic functions are well emulated in such transistors.

Interestingly, such temperature-dependent synaptic functions can be utilized to realize temperature induced spiking AND to OR logic transformation. Figure 5(a) shows a schematic diagram of an artificial neuron with branched dendrites. Such a neuron can process and integrate presynaptic inputs and transmit output signals through an axon to other neurons [40, 41]. As shown in Figure 5(b), an IGZO-based EDL neuromorphic transistor with two in-plane lateral gate electrodes, imitating the dendrite structure, is used to mimic presynaptic inputs integration at different temperatures. The G1 and G2 represent the two presynaptic input terminals, respectively. Figure 5(c) shows the two presynaptic input pulse trains applied on G1 and G2, respectively. The amplitude and duration time of a single spike are

1.0 V and 25 ms, respectively. Figures 5(d)–(f) show the output currents at 20°C, 40°C, and 60°C, respectively. Here, we set a threshold line with 30 nA of the postsynaptic current to define the state of “0” and “1” state. When the temperature is 20°C, the EPSCs are ~10.2, ~11.3, and ~21.5 nA triggered by the input pulse trains, respectively. None of them is more than 30 nA, so there is no response. Interestingly, when the temperature is 40°C, the EPSCs are ~13.9, ~14.9, and ~56.1 nA triggered by the input pulse trains, respectively. Only when both of the presynaptic driving inputs are applied to the transistor, the EPSC of ~56.1 nA exceeds 30 nA, and the “AND logic” is successfully obtained. When the temperature rises to 60°C, the EPSCs are ~58.6, ~60.0, and ~333.9 nA triggered by the input pulse trains, respectively. Obviously, all of the EPSCs are larger than 30 nA. Therefore, the “OR logic” is successfully obtained. Figures 5(g)–(i) further summarize the truth tables at 20°C, 40°C, and 60°C, respectively. As a result, when the temperature changes from 40°C to 60°C, “AND logic” to “OR logic” transformation is observed. This temperature-dependent spiking logic transformation is interesting for synaptic electronics and neuromorphic systems.

4 Conclusion

In summary, IGZO-based neuromorphic transistors with solid-state chitosan electrolyte as the gate dielectric films were fabricated. The temperature-dependent synaptic functions including EPSC, PPF, and dynamic filtering were successfully emulated. More interestingly, the temperature-dependent spiking logic was implemented in an IGZO-based neuromorphic transistor with dual in-plane gate electrodes. Spiking AND to OR logic transformation was realized only by changing the temperature. Our results provide an in-depth understanding of the temperature-induced synaptic functions and spiking logic transformation, which is interesting for building neuromorphic systems with high biological fidelity.

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