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A SiGe W-band frequency tripler with 10.5 dBm output power using harmonic suppression technique

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Dear editor,

The rapid development of silicon-based process has motivated great attention in mm-wave applications. Recently, W-band frequencies have become an appealing choice for various wireless applications, such as automotive radar, high data-rate communication, and high resolution imaging.

There are two traditional methods to generate local oscillator (LO) singals, implementing voltage-controlled oscillators (VCOs) operating at the desired frequencies directly or low-frequency VCOs followed with a multiplier chain [1–5]. The second scheme is more attractive in W-band frequencies for it can relax the designing challenge of the VCO and improve the phase noise. Furthermore, the fully differential architecture and the superior phase noise of a lower-frequency VCO make frequency tripler more suitable for the W-band signal generation than the frequency doubler. In this study, we present a high-performance frequency tripler utilizing unwanted harmonic suppression techniques and wideband transformer-based matching networks.

Circuit architecture. The frequency doubler is designed in a 0.13 μm SiGe BiCMOS process, featuring an f_T/f_{MAX} of 200/250 GHz. Figure 1(a) depicts the schematic of the frequency tripler, which is composed of a differential tripler core cascaded with a 3rd-order harmonic buffer. Considering both the output power and the dc power consumption, the widths of the transistors in the core and buffer are selected to be 8 μm and 10 μm, respectively. Based on the Maas' theory [6], the tripler core is biased near the pinch-off region with the optimum V_b of 0.82 V. The buffer stage is biased in class AB region with a current density of 0.6 mA/μm as a compromise between gain and output power.

Harmonic suppression technique. The high-order harmonic signals coupled from the output to the input port are harmful to the final desired harmonic power at the output [7]. To cope with this issue, harmonic reflectors are widely adopted in the frequency doubler design to suppress the harmonic signals at the input. However, conventional harmonic reflectors consisting of either 90° open stub or 180° short stub at the 2nd-order harmonic occupy a larger area and can only suppress the 2nd-order harmonic at the input port, which is not appropriate for the triper design.

In our design, two techniques are utilized to implement unwanted harmonic suppression at the input and boost the interested 3rd-order harmonic at the output. Firstly, a low pass filter composed of a shunt capacitor and a series inductance is inserted between the input balun and the tripler core, as shown in Figure 1(a). The capacitor is realized in a customized metal-oxide-metal structure for its high quality factor. The inductance is routed in a serpentine pattern to save the area. The low-pass (LP) filter leads the high-order harmonic signals to the ground and prevents power offsetting at the output [7]. Furthermore, the LP network is also responsible for the impedance transforming. Figure 1(b) depicts the trajectory of the input matching network. The conjugation of the optimum source impedance at the fundamental frequency (Z_{opt}*) and the input impedance at the 3rd-order harmonic frequency (Z_{in}*) are shown in Figure 1(b) as well. It is clear that with the help of the LP filter, the matching trajectory turns away from Z_{in}* and terminates near Z_{opt}*.

Another harmonic suppression technique aims to suppress the even-mode harmonics at the output, which is realized by cascading a 500 Ω resistor R_{rej} after the intersection of the common-base node N_b (see Figure 1(a)). Owing to the fully differential architecture, N_b can be regarded as a virtual ground for odd-mode harmonics. In practice, a bypass capacitor is typically placed at N_b to filter out the unbalanced components and ensure great grounding characteristics. However, the even-mode harmonics will also be boosted owing to the grounded N_b, and the even-mode stability will deteriorate. With the help of the series R_{rej}, the even-mode impedance looking outside the base node is quite high, and thus the even-mode, especially the 2nd-order, harmonics can be rejected. To validate the function of the proposed techniques, the harmonic power at the output of the tripler core with and without the above two harmonic suppression techniques is simulated (see Figure 1(c)). It is clear that the 3rd-order harmonic is considerably enhanced and the other unwanted harmonics are effectively suppressed thanks to the

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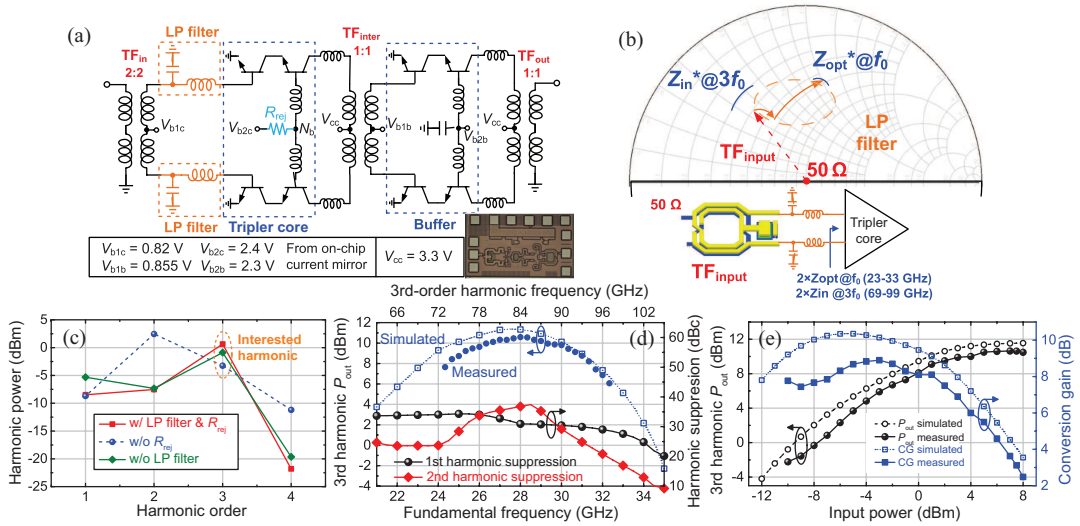

Figure 1 (Color online) (a) Schematic of the frequency tripler; (b) impedance transformation of the input matching network (the trajectory of the transformer is simplified); (c) simulated harmonic power at the output of the tripler core; (d) output power and harmonic suppression with the input power of 5 dBm; (e) output power and conversion gain with the fundamental frequency of 28 GHz.

proposed harmonic suppression techniques.

Wideband transformer-based matching network. To achieve broadband performance, transformers are utilized to implement single-ended to differential transforming and inter-stage matching. As high-order passive networks, transformers exhibit higher bandwidth than the single LC network. Moreover, the compact layout and presence of RF-virtual grounds enable the transformer-based balun to be a prior choice to the Marchand balun and LC balun. The inter-stage transformer TF_{inter} and output transformer TF_{out} with a turn ratio of 1:1 are realized by the top two thick metal layers while the third metal layer is indispensable for the input transformer TF_{in} with double rings. The imbalance issue is addressed by placing a grounded capacitor at the center node of the differential winding. Owing to the transformers, the insertion losses of the matching networks exhibit wideband frequency responses. It is noteworthy that the matching networks are deliberately designed at higher frequencies to compensate for the gain roll-off of the active devices.

Fabrication and measurement result. The overall chip occupies an area of 850 μm×520 μm including all pads (see Figure 1(a)). The chip is tested by on-wafer probing. Figure 1(d) depicts the measured and simulated 3rd-order harmonic output power versus input frequencies with an input power of 5 dBm. A peak output power of 10.5 dBm is achieved at 84 GHz and the 3-dB bandwidth is 19 GHz. Moreover, the measured unwanted fundamental and 2nd-order harmonics are suppressed by 30 dBc compared with the interesting 3rd-order harmonic from 76 to 90 GHz. Figure 1(e) shows that the frequency tripler achieves a peak output power of 10.5 dBm at 84 GHz. Compared with other state of the art designs operating in the similar frequency ranges [2–5,8], our circuit exhibits the highest output power with considerable bandwidth and unwanted harmonic rejection.

Conclusion. A W-band frequency tripler in a 0.13 μm SiGe process is presented in this study. Two techniques are implemented to boost the 3rd-order harmonic power at the output port, including utilizing an LP filter at the input and an extra resistor at the common-base node. The matching networks are based on transformers and exhibit wideband characteristics. The tripler achieves 10.5-dBm peak output power at 84 GHz with a 3-dB bandwidth of 19 GHz and more than 30-dBc unwanted harmonic suppression, which is appropriate for various W-band system architecture.

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References

1 Kang S, Chien J C, Niknejad A M. A W-band low-noise PLL with a fundamental VCO in SiGe for millimeter-wave applications. IEEE Trans Microw Theor Techn, 2014, 62: 2390–2404
2 Lee Y T, Hsiao Y H, Wang H. A 57-78 GHz frequency tripler MMIC in 65-nm CMOS. IEEE Microw Wireless Compon Lett, 2016, 26: 723–725
3 Yeh Y L, Chang H Y. A W-band wide locking range and low DC power injection-locked frequency tripler using transformer coupled technique. IEEE Trans Microw Theor Techn, 2013, 61: 860–870
4 Zhou P G, Chen J X, Li H B, et al. A high-efficiency E-band SiGe HBT frequency tripler with broadband performance. In: Proceedings of IEEE MTT-S International Microwave Symposium, Philadelphia, 2018. 690–693
5 Mazor N, Socher E. A SiGe distributed millimeter-wave frequency tripler. IEEE Microw Wireless Compon Lett, 2014, 24: 893–895
6 Maas S A. Nonlinear Microwave and RF Circuits. Norwood: Artech House, 2003
7 Wu K, Muralidharan S, Hella M M. A wideband SiGe BiCMOS frequency doubler with 6.5-dBm peak output power for millimeter-wave signal sources. IEEE Trans Microw Theor Tech, 2018, 66: 187–200
8 Chou M L, Chiu H C, Kao H L, et al. A 60-GHz CMOS frequency tripler with broadband performance. IEEE Microw Wireless Compon Lett, 2017, 27: 281–283