SCIENCE CHINA
Information Sciences

• LETTER •

April 2022, Vol. 65 149401:1–149401:3
https://doi.org/10.1007/s11432-020-2933-y

A centripetal collection image sensor (CCIS) based on back gate modulation achieving 1T submicron pixel

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Received 17 March 2020/Revised 20 May 2020/Accepted 25 May 2020/Published online 14 May 2021

Citation Liu L Q, Yu G H, Du G, et al. A centripetal collection image sensor (CCIS) based on back gate modulation achieving 1T submicron pixel. Sci China Inf Sci, 2022, 65(4): 149401, https://doi.org/10.1007/s11432-020-2933-y

Dear editor,

Image sensors have been rapidly developed for decades and widely used in many different fields [1, 2]. To achieve high resolution, the pixel size has been scaled down to 1 μm for mass production [3]. Nevertheless, the pixel size has to be further reduced to meet the growing demand for higher resolution. In CMOS image sensor (CIS), the pixel is composed of a photodiode, reset transistor, driver of the source-follower, and addressing transistor [4, 5]. However, the submicron pixel does not have enough space for too many transistors. To solve this problem, many studies have been done to develop one transistor (1T) image sensor [6]. By combining different pixel functions in one transistor, the number of in-pixel transistors can be minimized.

Utilizing the back gate modulation, ultra-thin body and buried oxide (UTBB) technology is a suitable choice to realize 1T image sensor. In UTBB image sensors, a deep depletion region or photodiode under the buried oxide (BOX) can be used to collect photo-generated carriers [7–9]. In these UTBB image sensors, the shallow trench isolation (STI) is used to separate the pixel cells and suppress electrical crosstalk. Nevertheless, when the pixel pitch of the UTBB image sensor shrinks down to submicron, there will be no enough space for STI. In this study, we propose a novel centripetal collection image sensor (CCIS) based on the UTBB structure to achieve a submicron single transistor pixel. Figure 1(a) shows the device structure of three adjacent CCIS pixels in the same row. A UTBB n-MOSFET is included in each pixel. The equivalent oxide thickness (EOT) is 1 nm, the silicon thickness is 6 nm and the channel length is 30 nm. Adjacent n-MOSFETs share a common drain and source to make the active area stay in one piece and avoid STI. To realize the centripetal charges collection, p-type storage wells (PS-well) and n-type isolation wells (NI-well) are formed alternately under the BOX to generate a centripetal electric field around the storage wells. The electric field can make the photo-generated carriers gather to the pixel center rather than diffuse to adjacent pixels. As a consequence, crosstalk suppression, the main function of STI, is achieved by the electric field. With 22 nm FD-SOI technology, the pixel structure can be realized by corresponding layout design. The operation period of the CCIS can be divided into RESET, EXPOSURE and READOUT stages. During the reset stage, −1 V is applied on Vn to forward bias the PN-junction. The accumulated charges of the last period are evacuated. During the exposure stage, 2 V is applied on Vn to reverse the PN-junction. Figure 1(b) shows the electrostatic potential distribution of the CCIS pixels during exposure stages. The arrows show the directions of the electric field around the p-type storage well. The electric field points to the center of the pixel. When the pixel is illuminated, the centripetal electric field can make the photo-generated holes drift to the p-type storage well and gather under the BOX, which raises the surface potential (Φs) at the well/BOX interface. Figure 1(c) shows the distribution of Φs under dark and after illumination. Owing to the back gate modulation, the Vth and Ion of the MOSFET will change after exposure. By detecting the Ion during the readout stage, the light signal can be evaluated. The shared drain and source structure are compatible with the CCIS array. The sources of all transistors in the same array are connected to a common electrode Vs and the drains of all transistors in one row are connected to the same bit line (BLi). By control of the word line (WLi) connected to the gate, only one transistor's signal is read out from every bitline at a time. By saving the area of STI, the pixel pitch of the CCIS can shrink down to 400 nm. To investigate the performance of the CCIS, TCAD tool Sentaurus is used.

In addition to the small pixel pitch, there is no STI between adjacent pixels in every row of the CCIS array. Therefore, the crosstalk suppression of the CCIS is of great significance. The crosstalk suppression mainly depends on the charges collection electric field. Figure 1(d) shows the ΔIon of seven adjacent pixels in the same row. The middle pixel 4

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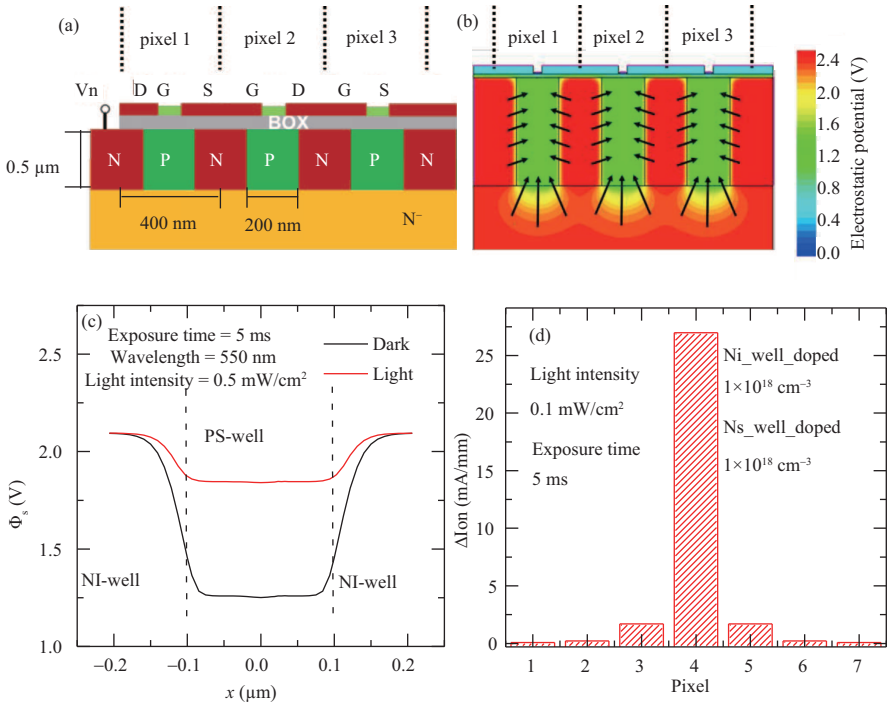

Figure 1 (Color online) (a) Device structure of the CCIS; (b) electrostatic potential distribution of the CCIS in exposure stage; (c) Φs distribution at well/BOX interface under dark and after illumination; (d) ΔIon of seven adjacent pixels in the same row after illumination on pixel4.

(P4) is illuminated and the rest are kept in dark. When the Ni_well_doped (doped concentration of the isolation well) is 1×10^{18} cm^{-3}, the ΔIon of P4 is about 27 μA/μm, and the ΔIon of P3 and P5 is about 1.7 μA/μm after illumination. The crosstalk between adjacent pixels is suppressed efficiently. The crosstalk rate is about 6.3%, which is comparable with the STI structure. However, the crosstalk suppression of the CCIS is strongly dependent on the doped concentration of isolation wells. When the Ni_well_doped reduces to 3×10^{17} cm^{-3}, the crosstalk suppression performance is seriously degraded. The crosstalk rate increases to 81.9%. When Ni_well_doped is 1×10^{18} cm^{-3}, the isolation wells are partly depleted. The potential barriers between storage wells of adjacent pixels are about 0.85 V. The depleted region at isolation wells expands as the Ni_well_doped becomes lower. The potential barriers between storage wells of adjacent pixels descend to 0.57 V. The lower Ni_well_doped can result in the degradation of crosstalk suppression by reducing the potential barriers between pixels. The diffusion of photo-generated charges occurring at the substrate also results in crosstalk. When Ni_well_doped is 1×10^{18} cm^{-3}, the depleted regions in the substrate of different pixels are separated. In this case, the photo-generated charges at the depleted region will gather into the in-situ pixel owing to the centripetal collection. The photo-generated charges outside the depleted region will be recombined before being collected by adjacent pixels. When Ni_well_doped reduces to 3×10^{17} cm^{-3}, the depleted regions in the substrate expand and join into one piece. This makes the photo-generated charges at the depleted region be able to diffuse to and be collected by adjacent pixels. Therefore, the isolation wells must be heavily doped to ensure crosstalk suppression.

The storage wells and the isolation wells are the keys to realize centripetal charges collection. Therefore, the well depth has great impact on the CCIS performance. With the Ns_well_doped (doped concentration of the storage well) and the Ni_well_doped fixed at 1×10^{18} cm^{-3}, the conversion gain of the CCIS increases from 21.4 μV/e$^-$ to 68.7 μV/e$^-$ when the well depth decreases from 0.5 μm to 0.1 μm. With different well depths, the quantum efficiency of the CCIS is almost equal. Therefore, the number of photo-generated charges will not change evidently with well depth. The photo-generated charges driven by the centripetal electric field will be accumulated in the storage well. With shallower well depth, the photo-generated charges can realize higher collection charge density, which finally results in higher conversion gain. The well doped concentration also has great impacts on the conversion gain of the CCIS. When the Ns_well_doped reduces to 1×10^{17} cm^{-3}, the conversion gain increases to 82.2 μV/e$^-$. With lower doped concentration, the storage well can be completely depleted and the electric field covers the whole storage well. As a result, the photo-generated charges driven by the electric field become more concentrated, which eventually achieves higher conversion gain.

The characteristics of the dark current of the CCIS also have a close relationship with the well structure. When well doped concentration is 1×10^{18} cm^{-3} and well depth is 0.5 μm, the dark current is about 890 e$^-$/s, which can reduce to 25 e$^-$/s when the Ns_well_doped reduces to 1×10^{16} cm^{-3}. With heavy well doped concentration, the centripetal electric field generated by the PN-junction is close to 3×10^5 V/cm. The strong electric field would accelerate the generation of the electron-hole pair, which finally results in the dark current. With a lightly doped storage well, the electric field covers the whole storage well and the electric field intensity decreases. Therefore, the dark current can be suppressed with a lightly doped storage well. The dark current can also be suppressed by reduced the well depth because the dark current is mainly generated by

the doped well.

Conclusion. In this study, a novel centripetal collection image sensor based on FDSOI technology has been investigated. In the CCIS image sensor array, adjacent pixels in the same row share a common drain and source to avoid STI. This can make the pixel pitch shrink down to 400 nm. The key of the CCIS is using a specific electric field to realize centripetal photo-generated charges collection and crosstalk suppression. To generate the centripetal electric field, a storage well and isolation well are designed. The well structure has great impact on the CCIS performance. The isolation wells must be heavily doped to ensure crosstalk suppression. The CCIS with shallow wells can realize higher collection charge density and lower dark current. When the storage wells are completely depleted, the electric field would cover the whole storage wells, which can improve the conversion gain and suppress dark current. The CCIS can realize up to 62% quantum efficiency. According to the layout design, the fill factor of the CCIS is about 42%. The efficient photoelectric conversion and good crosstalk performance of the CCIS are demonstrated by TCAD simulation. It presents great potential for higher-resolution applications.

Acknowledgements This work was supported in part by National Key R&D Plan (Grant No. 2016YFA0202101) and National Natural Science Foundation of China (Grant No. 61674008).

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