SCIENCE CHINA
Information Sciences

April 2022, Vol. 65 140402:1–140402:15
https://doi.org/10.1007/s11432-021-3401-6

• RESEARCH PAPER •
Special Focus on Brain Machine Interfaces and Applications

A 124 dB dynamic range sigma-delta modulator applied to non-invasive EEG acquisition using chopper-modulated input-scaling-down technique

Kaiquan CHEN[1], Mingyi CHEN[1*], Longlong CHENG[2], Liang QI[1], Guoxing WANG[1] & Yong LIAN[1]

[1]*Department of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai* 200240*, China;*
[2]*China Electronic Cloud Brain (Tianjin) Technology Co.,Ltd., Tianjin* 300309*, China*

Received 25 September 2021/Revised 17 November 2021/Accepted 23 December 2021/Published online 9 March 2022

Abstract With the advancement of brain science in recent years, the non-invasive brain-computer interfaces (BCIs) based on electroencephalogram (EEG) acquisition have been widely adopted in various brain-inspired applications. The acquisition of multi-channel microvolts EEG signals corrupted by the motion artifacts (MAs) of up to several volts poses enormous challenges to the design of analog front-end (AFE), especially the analog-to-digital converter (ADC), which is necessary to achieve low noise, wide dynamic range (DR), high accuracy as well as low power. In this paper, a wide DR $\Sigma\Delta$ modulator with chopper-modulated input-scaling-down (CM-ISD) technique has been proposed to deal with large input offset while extending dynamic range. Fabricated in 180 nm CMOS technology, the prototype occupies a core area of 0.32 mm^2. With a 40 Hz input signal and 125 Hz Nyquist bandwidth, the measured signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) are 117 and 110 dB, respectively. Thanks to the proposed CM-ISD technique, the modulator is capable of withstanding a full-scale (4.5 V_{pp}) input whereas the measured DR has been extended from 99 to 124 dB. The power consumption is 2.75 mW under 5 V supply voltage, corresponding to 170.6 dB Schreier figure-of-merit (FoM_S). The multi-channel EEG acquisition has been demonstrated based on the proposed modulator, showing its potential in advanced non-invasive BCI systems.

Keywords analog-to-digital converter (ADC), $\Sigma\Delta$ modulator, brain computer interface (BCI), electroencephalogram (EEG), dynamic range (DR), motion artifacts (MA)

Citation Chen K Q, Chen M Y, Cheng L L, et al. A 124 dB dynamic range sigma-delta modulator applied to non-invasive EEG acquisition using chopper-modulated input-scaling-down technique. Sci China Inf Sci, 2022, 65(4): 140402, https://doi.org/10.1007/s11432-021-3401-6

1 Introduction

With the acceleration of brain research in recent years, brain-computer interfaces (BCIs) have attracted much attention due to their capability in the diagnosis and treatment of brain diseases as well as brain-inspired applications [1–5]. According to the way of brain signal acquisition, BCIs can be divided into two independent technical paths: invasive and non-invasive. Non-invasive BCI based on the electroencephalography (EEG) signal is preferred for most applications due to its low cost and good user acceptance. However, the low-frequency (0.5–50 Hz) EEG is the weakest bio-potential signal with extremely low amplitude (1–100 μV) [6], which is inevitably affected by the circuit noise as well as external environmental interference, such as powerline interference at 50/60 Hz. Meanwhile, during the non-invasive EEG acquisition through dry electrodes, the recorded EEG signal is susceptible to the motion artifacts (MAs) caused by relative movements between the skull and the electrodes. The amplitude of the MA is normally much (over 5–6 orders of magnitude) larger than that of the EEG signal [7–10]. Therefore, in order to amplify the weak EEG signal while enabling the back-end digital-signal-processing (DSP) to practically remove the MA [11], the EEG acquisition circuit, e.g., the analog front-end, should be built

* Corresponding author (email: mychen@sjtu.edu.cn)

with low noise, high accuracy, high linearity, and wide dynamic range (DR). Furthermore, to improve the spatial resolution of the non-invasive BCI, multi-channel EEG acquisition is preferred, which introduces additional restrictions on power consumption, especially for wearable devices. These requirements pose enormous challenges to the design of analog-to-digital converter (ADC), which is necessary to have ultra-high resolution (up to 24-bit), wide DR ($\geqslant$ 120 dB) as well as low power for multi-channel non-invasive EEG acquisition.

In the past decades, high-performance ADCs applied in EEG acquisition have been widely investigated. The Nyquist-rate successive-approximation-register (SAR) ADC is the most popular one due to its high power efficiency and small area [12]. The additional digital calibration technique is usually required to achieve high resolution. In [13], a 14-bit SAR ADC has been implemented with digital calibration to improve the signal-to-noise ratio (SNR). However, even with the most advanced digital calibration technique, the noise of the internal comparator fundamentally limits its resolution to 16 bits [14]. Incremental ADC (IADC) provides another way of Nyquist-like conversion, which has been widely adopted in high-resolution applications because of its low latency, easy multiplexing, and simple digital filtering properties. Nevertheless, IADC is normally applied to convert signals with extremely low frequency, or even DC signal, thereby impeding its application in multi-channel EEG acquisition, which requires higher signal bandwidth. Oversampling $\Sigma\Delta$ ADC is another widely adopted architecture, which can be divided into two categories of continuous-time (CT) and discrete-time (DT). A CT $\Sigma\Delta$ modulator with 300 $\mathrm{mV_{pp}}$ linear input range and 80.4 dB signal-to-noise and distortion ratio (SNDR) is presented in [15], while a 3rd-order $\mathrm{G_m}$-C CT $\Sigma\Delta$ modulator with a 5-bit SAR quantizer which improves the DR to 92.3 dB is proposed in [16]. Although the intrinsic anti-aliasing feature of the CT $\Sigma\Delta$ ADC reduces the power consumption [17], the sensitivity to the variation of the process, voltage and temperature makes it less attractive to be applied to robust and long-term non-invasive EEG acquisition [18]. Voltage-controlled oscillator (VCO)-based ADC appeared in recent years, which has benefits in elevating SNR because of the intrinsic noise shaping [19, 20]. A scalable 2nd-order VCO-only $\Sigma\Delta$ ADC achieving 92.3 dB DR, 110.3 dB spurious-free dynamic range (SFDR) in a 1 kHz bandwidth has been implemented in [21]. A distortion-free VCO-based front-end achieving 128 dB SFDR and 95.1 dB DR with a differential pulse code modulation (DPCM) technique has been exploited in [22]. However, the noise is the fundamental problem that limits its DR [23]. Considering all the aforementioned aspects, DT $\Sigma\Delta$ ADC [24] is the best candidate to achieve low noise, high resolution and DR [25] in robust non-invasive EEG acquisition applications. As the most critical block in the DT $\Sigma\Delta$ ADC, the performance of the $\Sigma\Delta$ modulator usually dominants the final performance of the whole ADC. Nevertheless, it is still the most challenging task up to date to realize a $\Sigma\Delta$ modulator over 120 dB DR while consuming no more than several milliwatts power within a Nyquist bandwidth of hundreds of Hertz.

In this study, we propose a DT $\Sigma\Delta$ modulator suitable for non-invasive EEG acquisition based on the cascade of integrators feedforward and feedback (CIFF-B) architecture [26, 27]. High DR of 124 dB has been achieved at the power consumption of 2.75 mW by involving the following techniques. Firstly, an innovative chopper-modulated input-scaling-down (CM-ISD) technique has been proposed to attenuate the input amplitude by a factor of 5/8, which makes the maximum input of the modulator extend to full-scale without inducing saturation or instability of the loop. Furthermore, the scaling-down factor is compensated in the decimation filter without reducing the signal gain. Secondly, the mismatch of the feedback digital-to-analog converter (DAC) is reduced by the dynamic-weighted-averaging (DWA) technique [28]. Finally, a cross-coupling positive feedback technique has been employed in the feedforward Miller compensation (FFMC) transconductance amplifier (OTA) so that the excessive harmonic distortion and integration leakage due to the effect of the parasitic capacitance of input transistors can be effectively eliminated. The prototype has been fabricated with 180 nm CMOS technology, occupying an area of 0.32 $\mathrm{mm^2}$. With a 40 Hz input signal frequency and 125 Hz Nyquist bandwidth, the measured SNR and SNDR are 117 and 110 dB, respectively. Thanks to the input CM-ISD technique, the modulator is capable of withstanding full-scale differential input of 4.5 $\mathrm{V_{pp}}$ whereas the measured DR has been improved by 25 dB. The current consumption is 550 μA, corresponding to 170.6 dB Schreier figure-of-merit ($\mathrm{FoM_S}$). The real EEG signal measurement has been carried out to demonstrate its capability in non-invasive BCI systems.

The rest of the paper is organized as follows: Section 2 introduces the architecture of the proposed $\Sigma\Delta$ modulator; Section 3 illustrates the detailed circuit implementation; Section 4 shows the experimental results; and the conclusion is drawn in Section 5.

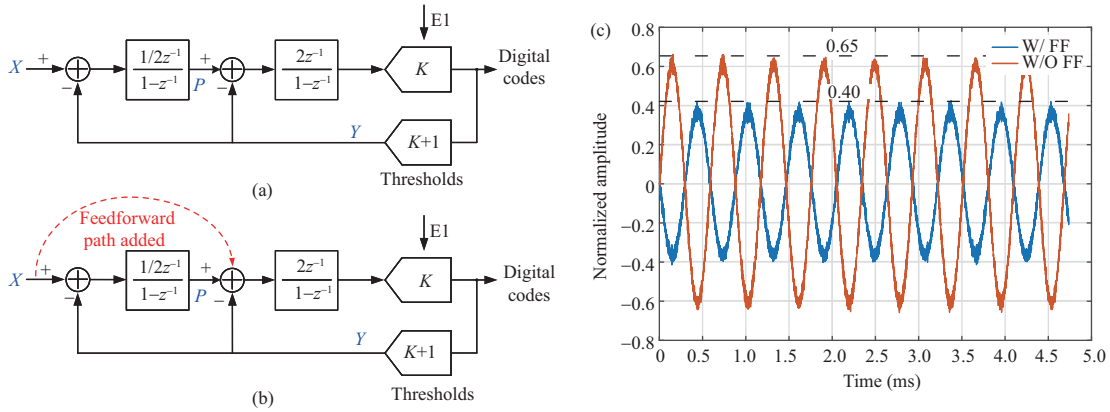


Figure 1 (Color online) (a) CIFB architecture; (b) CIFF-B architecture; (c) transient simulation results of the output swing of the first stage integrator with/without feedforward path.

2 Architecture of the proposed modulator

2.1 Architecture overview and feedforward path

The proposed modulator utilizes a 2nd-order 3-bit architecture with a sampling frequency of 1.024 MHz, corresponding to an over-sampling ratio (OSR) of 4096 within 125 Hz Nyquist bandwidth. The behavior simulation shows that over 159.3 dB signal-to-quantization-noise ratio (SQNR) can be achieved. Therefore, the keys to extending the DR are to minimize the circuit noise (i.e., thermal and flicker noise) and to avoid harmonic distortion with large input amplitude.

In order to reduce the harmonic distortion, it is critical to limit the output swing of the first integrator. Since the input of the first integrator cannot be shaped by the modulator loop, it probably leads to a large output swing when the input amplitude is large. In the conventional cascade of integrators feedback (CIFB) architecture (Figure 1(a)), the output of the modulator (Node Y) can be expressed by the following equation:

$$Y = Xz^{-2} + \varepsilon_Q(1 - z^{-1})^2. \tag{1}$$

Therefore, the output of the first integrator (Node P) can be expressed as

$$P = \frac{(X - Y)z^{-1}}{2(1 - z^{-1})} = X\frac{z^{-1}(1 + z^{-1})}{2} + \varepsilon_Q\frac{z^{-1}(1 - z^{-1})}{2}. \tag{2}$$

The first item is equal to the average of two consecutive sampled inputs, while the second item is equal to the high-pass filtered counterpart of the quantization error. With a multilevel quantizer, the amplitude of node P is mainly determined by the first item. As a result, the output swing will be high with a large input amplitude, which might lead to large harmonic distortion.

The feedforward path is an effective way to reduce the output swing of the first integrator. Figure 1(b) shows the modulator with the feedforward path. If the input average value of the second integrator is zero, its output is bounded. With the feedforward path, the input of the second integrator consists of three parts: $(-Y)$, P and X, so it must be ensured that $(-Y) + P + X = 0$. Therefore, P is close to the quantization error, which can be very small with a multilevel quantizer. Nodes Y and P can be expressed as

$$Y = X[z^{-2} + 2z^{-1}(1 - z^{-1})] + \varepsilon_Q(1 - z^{-1})^2, \tag{3}$$

$$P = \frac{(X - Y)z^{-1}}{2(1 - z^{-1})} = X\frac{z^{-1}(1 - z^{-1})}{2} + \varepsilon_Q\frac{z^{-1}(1 - z^{-1})}{2}. \tag{4}$$

Comparing (2) and (4), it can be shown that the swing at node P is significantly reduced with an additional feedforward path. Figure 1(c) shows the comparison of the transient simulation results with/without the feedforward path. The output swing of the first integrator is reduced by 38% with the feedforward path. It is noteworthy that the additional feedforward path changes the signal transfer function (STF) from a simple double delay to the following equation:

$$\mathrm{STF}(z) = z^{-2} + 2z^{-1}(1 - z^{-1}). \tag{5}$$

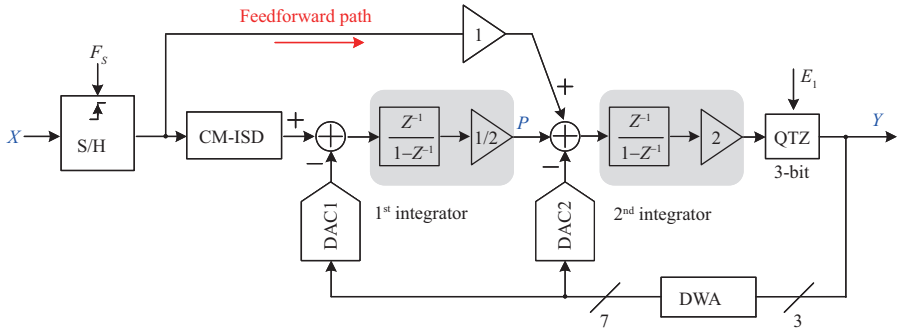


Figure 2 (Color online) Detailed architecture of the proposed ΣΔ modulator.

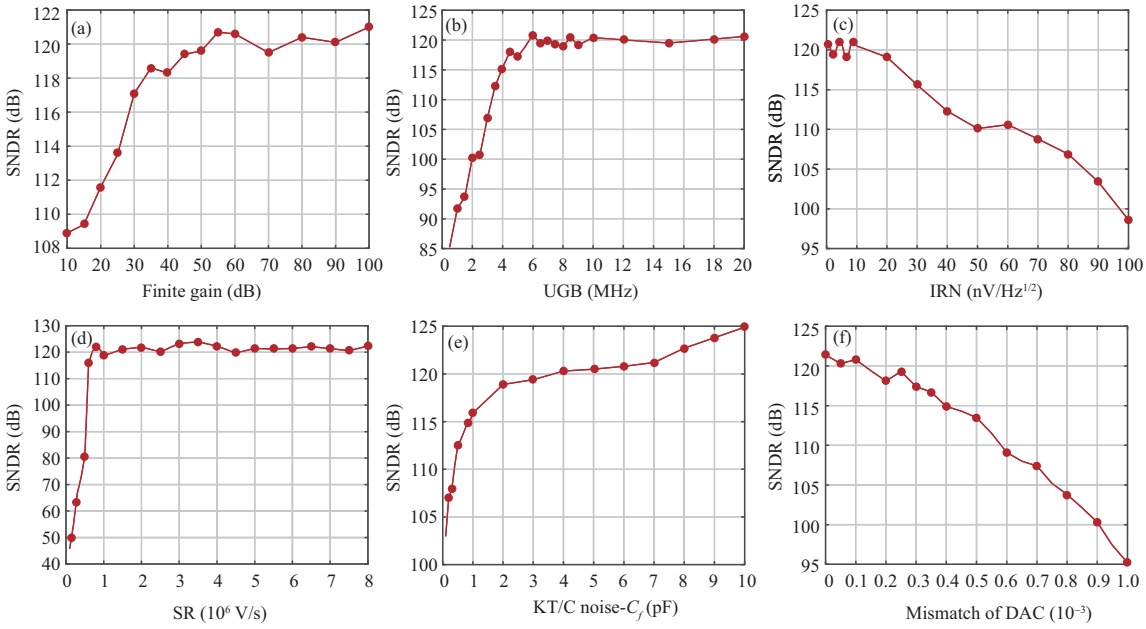


Figure 3 (Color online) Impacts of circuit non-idealities to SNDR including (a) finite gain, (b) unity-gain-bandwidth, (c) input-referred-noise, (d) slew-rate, (e) KT/C noise and (f) accuracy of the feedback DACs.

The introduced error due to the second item can be compensated in the digital decimation filter.

2.2 Analysis of circuit non-ideality

Figure 2 shows the block-level architecture of the proposed modulator. The analog input is sampled and then scaled-down with the CM-ISD block preceding the loop filter. The loop filter consists of two stages of switched-capacitor (SC) integrators and a 3-bit quantizer (QTZ). The coefficients of the first and second stages are 1/2 and 2, respectively. An additional path with unity-coefficient-value is feedforward to the output of the first stage. A 3-bit quantizer is adopted, with two DACs feedbacking to each stage of the integrator. DWA technique is employed to reduce the mismatch of the DAC capacitor array. To form a complete ΣΔ ADC, a 3-order cascaded-integrator-comb (CIC) decimation filter following modulator should be added, which downsamples the data and eliminates the quantization noise beyond the Nyquist bandwidth.

The behavior simulation is conducted to evaluate the impacts of the circuit non-idealities on the SNDR. These non-idealities include finite gain and unity-gain-bandwidth (UGB) of the OTA, input-referred-noise (IRN) and slew-rate (SR) of the OTA, KT/C noise of the sampling switches and mismatch of the feedback DACs.

Figure 3 shows the simulation results, from which the circuit-level design specifications can be worked out. Among these non-idealities, we found that the noise (KT/C noise as well as the OTA's IRN) and DAC mismatch have a dominant impact on the SNDR. As a result, the value of the sampling capacitance should be sufficiently large ($\geqslant$4 pF) whereas the OTA's IRN should be minimized ($\leqslant$30 nV/Hz$^{1/2}$). The

Table 1 The impact of circuit non-idealities to SNDR

Non-ideality	Design specifications	Unit
KT/C noise	$\geqslant$4	pF
IRN	$\leqslant$30	nV/Hz$^{1/2}$
UGB	$\geqslant$5	MHz
Finite gain	$\geqslant$55	dB
SR	$\geqslant 10^6$	V/s
DAC mismatch	$\leqslant$100	ppm

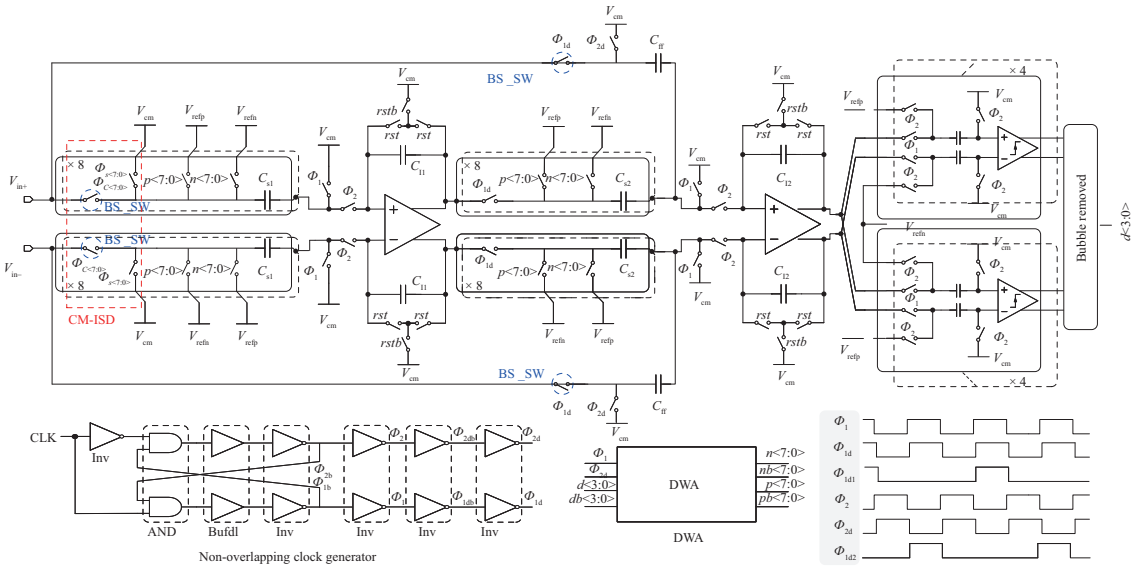


Figure 4 (Color online) Top-level schematic of the ΣΔ modulator.

flicker noise of the OTA should also be carefully treated to prevent dominating the IRN. Meanwhile, the DAC mismatch should be less than 100 ppm, which is not a practical value for the on-chip capacitor with an acceptable area. Therefore, the DWA technique is employed to reduce the mismatch of the DAC capacitor array. Table 1 lists these specifications to ensure 120 dB SNDR.

3 Circuit implementation

Figure 4 shows the top-level schematic of the proposed ΣΔ modulator. The two stages of SC integrators are coordinated by the clock from the non-overlapping clock generator, with the coefficients determined by the capacitance ratio of $C_{\rm S}/C_{\rm I}$. The two feedback DACs are realized with the capacitor array controlled by the thermometer codes from the 3-bit quantizer as well as the DWA. All the reference voltages are from the on-chip low-noise reference generator.

3.1 Chopper-modulated input-scaling-down

Figure 5 shows the schematic and timing diagram of the proposed CM-ISD. The scaling down factor of 5/8 is introduced to optimize the STF. The simplest implementation is to share the 8 capacitors for sampling and feedback DAC, respectively, while using 5 capacitors for sampling to generate the scaling down factor of 5/8 and 8 capacitors for feedback DAC. The sampling capacitors have been divided into two groups (each group with 5 capacitors) to eliminate the coefficient mismatch: the first group includes $C_{\rm S1}$–$C_{\rm S5}$, whereas the second group includes $C_{\rm S4}$–$C_{\rm S8}$. The chopper modulation is introduced to alternatively switch the two groups (each group with 5 capacitors) to eliminate the coefficient mismatch. Each time the input is sampled, one group of the sampling capacitors is connected to the input and stores the charge. Then the charge is transferred to the output through $C_{\rm I}$ in the following integration phase. Since the capacitance value of $C_{\rm S}$ is equal to 1/8 of $C_{\rm I}$, the integration coefficient is equal to $5/8(1+\delta_r+\delta_s)$, where δ_r is the standard deviation of random mismatch between $C_{\rm S}$ and $C_{\rm I}$ dependent on the area of the unit

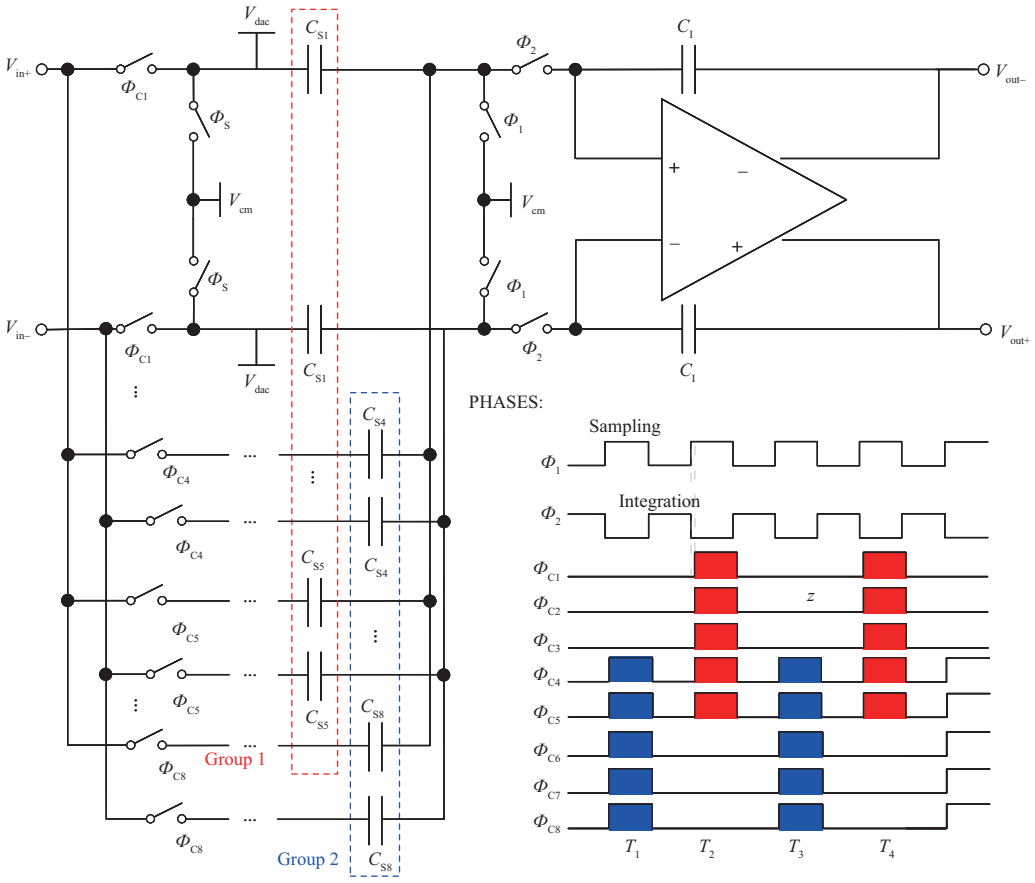


Figure 5 (Color online) Schematic and timing diagram of the proposed CM-ISD.

capacitor, and δ_s is the standard deviation of the systematic mismatch dependent on the layout matching degree between $C_{\rm S}$ and $C_{\rm I}$. In the subsequent sampling phase, with the control of the CM, the other group of the sampling capacitors is connected to the input, and the stored charge is transferred to the output in the same way. The integration coefficient in this phase is equal to $5/8(1+\delta_r-\delta_s)$, where the δ_r remains the same but the systematic mismatch has the opposite sign because of the adopted common-centroid layout of $C_{\rm I}$ with regard to the two groups of $C_{\rm S}$. Therefore, through the alternative connection of both capacitor groups, the integration coefficient will be averaged to around $5/8(1+\delta_r/\sqrt{2})$, where the random mismatch is reduced while the systematic mismatch is first-orderly cancelled. In this manner, the coefficient sensitivity to the capacitance mismatch is reduced.

Furthermore, the scaling down factor of 5/8 introduced by the CM-ISD allows the modulator to withstand full-scale input without loop saturation or instability, leading to extended DR. In addition, the coefficient mismatch is averaged to narrow the standard deviation, which minimizes the mismatch-induced error for improved accuracy. The drawback of the scaling down is an increase in the input-referred noise of the modulator by a factor of 3/5. This can be addressed by the precedent IA.

3.2 SC integrator and OTA

Figure 6 shows the schematic of the SC integrator and its small signal equivalent model. For simplicity, we hereby draw the single-ended version instead of the fully-differential one in real implementation. The integrator works as follows: in ϕ_1, the input voltage is sampled onto the bottom plate of $\rm C_S$ and the charge is stored. While in ϕ_2, the charge is transferred to $\rm C_I$ for the integration. The bottom plate of $\rm C_S$ is disconnected in advance to ϕ_1 and ϕ_2, so that the charge injection effect could be effectively reduced. Since the non-linearity due to the sampling error cannot be shaped by the modulator loop, it is critical to improve the linearity of the sampling switch. By adopting the bootstrap switch [29] and carefully sizing the switch, the settling-error-induced non-linearity can be well minimized. As shown in Figure 7, the bootstrap switch can obtain 122.0 dB SNDR (fin = 40 Hz@BW = 125 Hz).

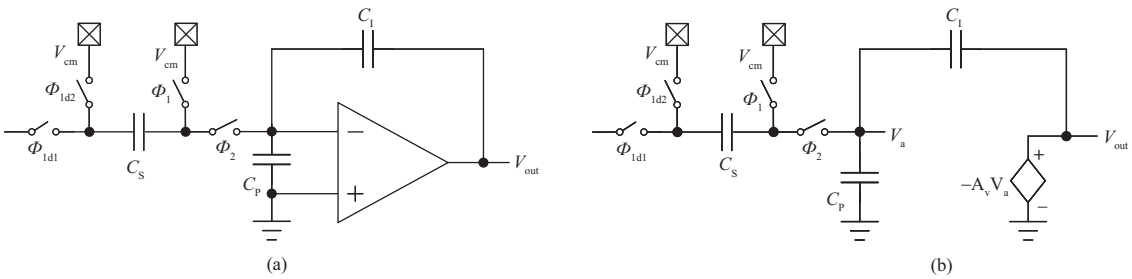


Figure 6 (a) Schematic of the SC integrator and (b) its small signal equivalent model.

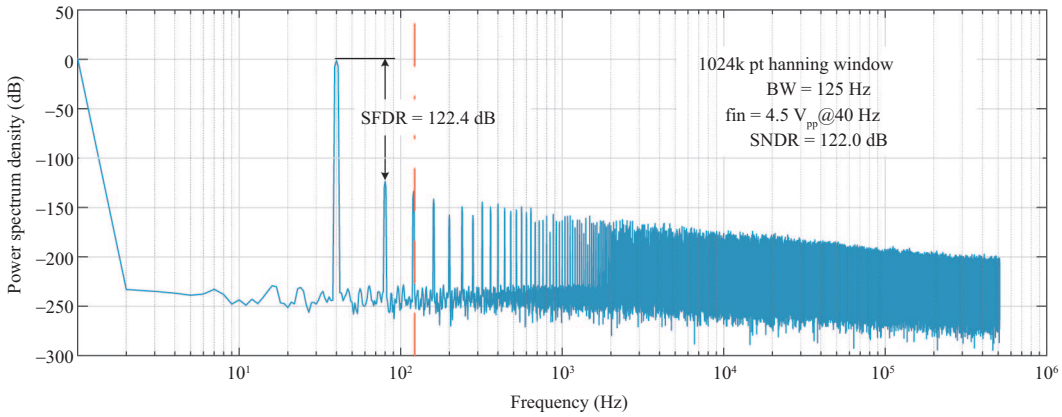


Figure 7 (Color online) Simulation result of the bootstrap sampling switch.

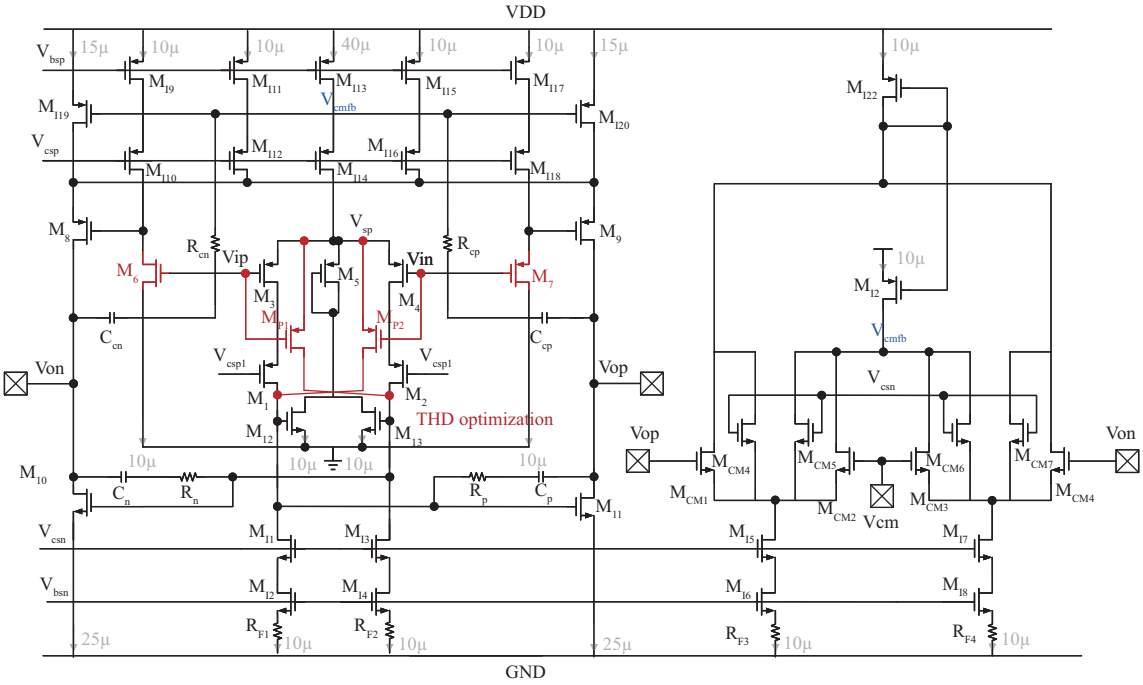


Figure 8 (Color online) Schematic of the OTA in the integrator.

Figure 8 shows the detailed schematic of the OTA based on FFMC architecture [30]. Compared with the conventional Miller compensation, the additional feedforward path formed by transistors M_8 and M_9 introduces a left-half-plane (LHP) zero; thereby the phase lag can be effectively compensated with less

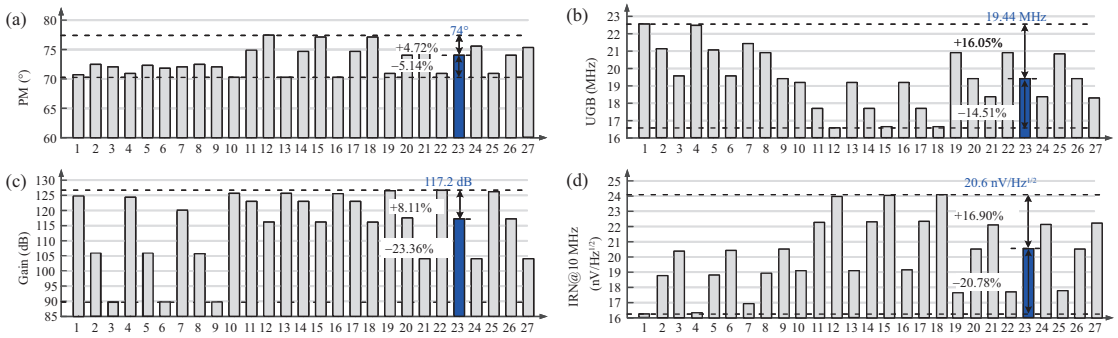


Figure 9 (Color online) The simulation results of the (a) PM, (b) UGB, (c) Gain and (d) IRN of the Opamp under different PVT conditions.

power consumption overhead. The position of the introduced LHP zero can be expressed as

$$z \approx -\frac{g_{m1}g_{m2}}{sC_{\rm c}(g_{m3}-g_{m1})} = -f_{\rm UGB}\frac{g_{m2}}{(g_{m3}-g_{m1})}, \tag{6}$$

where g_{m1} and g_{m2} denote the equivalent transconductance of the first and second stage of the operational amplifier, g_{m3} is the transconductance of the feedforward path and $C_{\rm c}$ is the compensation capacitance. Therefore the zero frequency can be exactly fixed by relative sizing of the transistors. In contrast to the FFMC OTA proposed in [30], we add two source followers ($\rm M_6$ and $\rm M_7$) from the input to the feedforward stage ($\rm M_8$ and $\rm M_9$) to extend the output swing. Without $\rm M_6$ and $\rm M_7$, to ensure the saturation of $\rm M_8$ and $\rm M_9$, the maxim output swing is given by

$$V_{\rm out,max} = V_{\rm in,DC} + |V_{\rm thp}|, \tag{7}$$

where $V_{\rm in,DC}$ is the input DC bias voltage and $V_{\rm thp}$ is the threshold voltage of the $\rm M_8$ and $\rm M_9$. With the added $\rm M_6$ and $\rm M_7$, the maxim output swing is extended to

$$V_{\rm out,max} = V_{\rm in,DC} + \left|V_{\rm GS6,7}\right| + |V_{\rm thp}| \cong V_{\rm in,DC} + \left|V_{\rm DSAT6,7}\right| + 2\,|V_{\rm thp}|, \tag{8}$$

where $V_{\rm DSAT6,7}$ is the overdrive voltage of $\rm M_6$ and $\rm M_7$. The distortion of $\rm M_8$ and $\rm M_9$ will be effectively avoided with an increased maximum output swing so that the linearity of the SC integrator can be improved as well. To avoid the non-linearity of integrator induced by the input parasitic capacitance of OTA, positive feedback composed of two cross-coupled transistors $\rm M_{P1}$ and $\rm M_{P2}$ has been added. The positive feedback presents a 'negative' capacitance that partially cancels the parasitic capacitance $C_{\rm P}$ mainly formed by the gate-to-drain capacitance ($C_{\rm GD}$) of $\rm M_3$ and $\rm M_4$. As given in [31], the $\rm HD_3$ of the modulator can be expressed by

$$\rm HD_3 = \frac{k_3A^2}{4k_1^3}|NTF(z)| = \frac{k_3A^2}{4k_1^3}\left|\frac{1}{1+2K_{I1}\left(\frac{z^{-1}}{1-z^{-1}}\right)^2+2\left(\frac{z^{-1}}{1-z^{-1}}\right)}\right|, \tag{9}$$

where k_1 and k_3 are coefficients of the first and third items in the Taylor expansion and $K_{\rm I1}$ is reciprocal of the integration coefficient which can be expressed by

$$K_{\rm I1} = C_{\rm I}/(C_{\rm S}+C_{\rm P}). \tag{10}$$

It is obvious from (9) and (10) that $C_{\rm P}$ reduces $K_{\rm I1}$, leading to larger $\rm HD_3$. With the introduction of 'negative' capacitance $C_{\rm PN}$ formed by $M_{\rm P1}$ and $M_{\rm P2}$, $K_{\rm I1}{}'$ can now be expressed by

$$K_{\rm I1}{}' = C_{\rm I}/(C_{\rm S}+C_{\rm P}-C_{\rm PN}). \tag{11}$$

As a result, $\rm HD_3$ can be reduced, e.g., 10-time reduction in $C_{\rm P}$ improves $\rm HD_3$ by 13 dB.

Figure 9 shows the simulation results of OTA. The specification of Gain, UGB, PM, IRN has been simulated under 27 conditions including different process corners (ss/tt/ff), voltage (4.8/5/5.2 V) and temperature (−40/40/85 °C). When driving 4 pF load capacitance, the OTA achieved 119.7-dB gain,

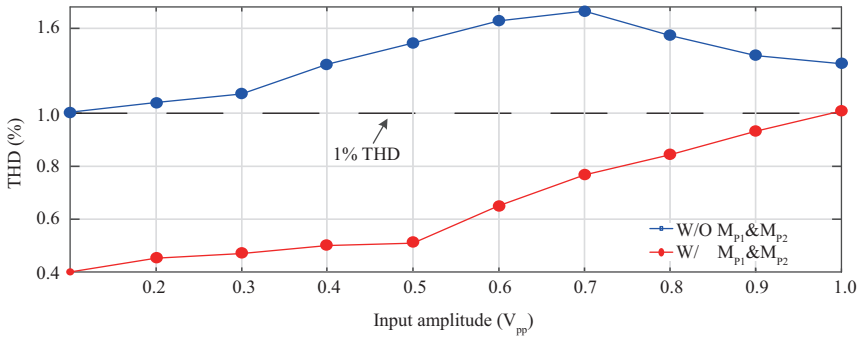


Figure 10 (Color online) THD (%) versus input amplitude (V_{PP}) with/without M_{P1} and M_{P2}.

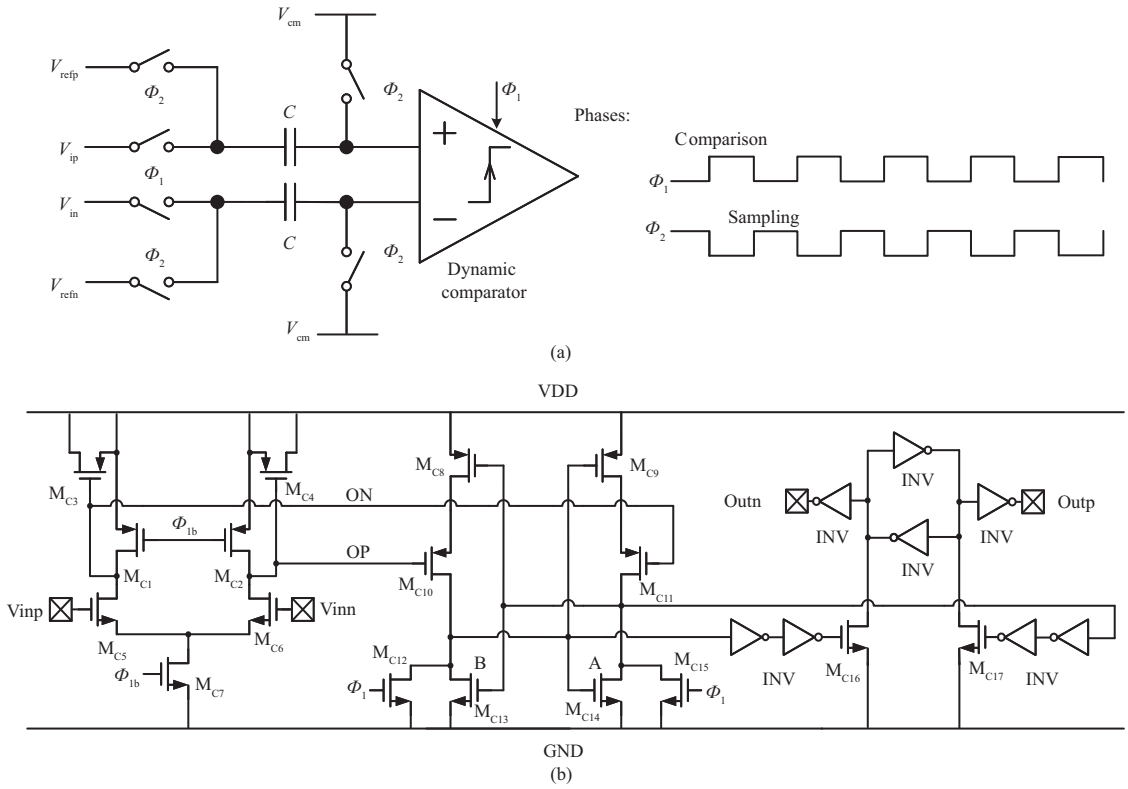


Figure 11 Schematic of (a) the SC comparator and (b) the dynamic comparator.

18.95-MHz unity-gain-bandwidth and 74.6° phase-margin with 20.7-nV/Hz$^{1/2}$@10 MHz input-referenced-noise, dissipating 750.5-μW power under 5 V supply voltage. The worst-case performance should be guaranteed to meet the requirements listed in Table 1. In addition to minimizing the IRN, the flicker noise of the OTA is well controlled by increasing the gate area of the M_3 and M_4, as well as by the insertion of source degeneration resistors R_{F1} and R_{F2}. The simulation results show the input referred RMS noise integrating from 0.5 to 100 Hz is 1.5 μV. Figure 10 shows the simulated total-harmonic-distortion (THD) without/with M_{P1} and M_{P2}, which indicates the 1% THD linear-input-range is increased from 100 mV_{pp} to 1 V_{pp}. In summary, the SC integrator based on the OTA achieves an optimized performance in terms of noise, accuracy, linearity and DR through an elaborate circuit design without sacrificing other specifications of the OTA.

3.3 Multi-bit SC quantizer

Figure 11(a) shows the schematic and timing diagram of the SC comparator. It works as follows: When ϕ_2 is high, the top plates of the sampling capacitors are connected to $V_{\rm cm}$, while the reference voltage ($V_{\rm refp}$ and $V_{\rm refn}$) are sampled to the bottom plates. Therefore, the stored differential charge is $C\cdot(V_{\rm refp}-V_{\rm refn})$.

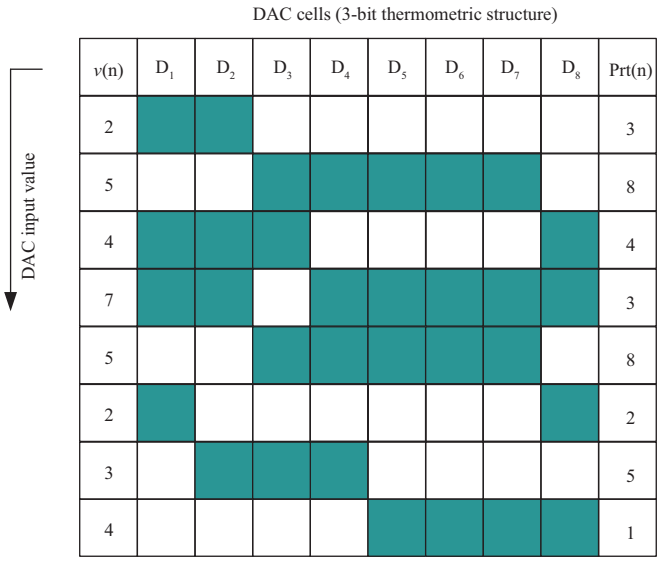


Figure 12 (Color online) Illustration of the DWA algorithm. The left-most column is the input data sequence, the right-most column is the 'pointer' sequence.

When ϕ_1 is high, the input voltages $V_{\rm ip}$ and $V_{\rm in}$ are sampled to the top plates. Due to the law of charge conservation, the differential inputs of the comparator are equal to $(V_{\rm ip} - V_{\rm in}) - (V_{\rm refp} - V_{\rm refn})$. By setting different reference voltage levels for eight parallel SC comparators, a 3-bit quantizer is formed. Since the offset of the comparator is high-pass filtered by the modulator loop, it does not introduce significant errors in the final results. In other words, offset cancellation is not required. However, to prevent the error due to offset-induced 'bubble' in the thermometer code, a 'bubble' removal circuitry has been added.

Figure 11(b) shows the detailed schematic of the dynamic comparator. When ϕ_1 is low, the comparator is in the 'Reset' phase by turning off the $\rm M_{C7}$ while turning on $\rm M_{C1}$ and $\rm M_{C2}$. In this phase, nodes OP and ON are pulled up to $V_{\rm DD}$. When ϕ_1 is high, the comparator is in the 'Comparison' phase, i.e., nodes OP and ON begin discharging. The discharging rate is dependent on the differential inputs level. For example, assume $(V_{\rm ip} - V_{\rm in}) > (V_{\rm refp} - V_{\rm refn})$, and then the discharging rate of ON will be faster than OP. As long as the voltage difference between ON and OP surpasses the threshold of the dynamic latch formed by $\rm M_{C8}$–$\rm M_{C14}$, the comparison result will be latched.

3.4 Dynamic-weighted-averaging

DWA [32] has been employed to reduce the mismatch of the feedback DAC capacitance to be less than 100 ppm. In the DWA algorithm, the selection of the eight DAC cells (3-bits) is based on the input data sequence and the currently used cells. For example, we assume that the input sequence is '2, 5, 4, 7, 5, 2, 3, 4' as shown in Figure 12. The colored grids represent the currently used DAC cells, while the white grids represent the unused ones. The elements are selected in a round-robin manner so that each element has the same probability to use. Therefore, the mismatch in the case of multiple cells can be quickly averaged, and the DAC mismatch can be effectively 1st-ordered shaped and pushed to high frequency. The DAC matching error [33, 34] can now be expressed as

$$\mathrm{DAC}_{\rm error} = \left(\frac{\pi^2}{3\cdot \mathrm{OSR}^3}\cdot\frac{\sigma_\alpha^2\cdot\left(1-\frac{1}{M}\right)^2\cdot M}{12}\right)^{1/2}, \tag{12}$$

where OSR is the oversampling ratio and M is the number of cells in the DAC. σ_α is the standard deviation of the random mismatch error of the unit cell. With OSR = 4096, $M = 8$, $\sigma_\alpha = 0.25\%$, the DAC matching error can be improved to be less than $1.24\mathrm{e}^{-2}$ ppm in theory, which provides sufficient safety margin according to Table 1.

Figure 13 shows the block diagram of the DWA circuit. The 3-bit full adder sums the kth and $(k+1)$th binary codes from the 3-bit quantizer, where the carry $C_{\rm o}$ of the lower adder is given to the $C_{\rm in}$ of the upper adder. If the summation result is larger than 8, the Modulo operation is implemented so that

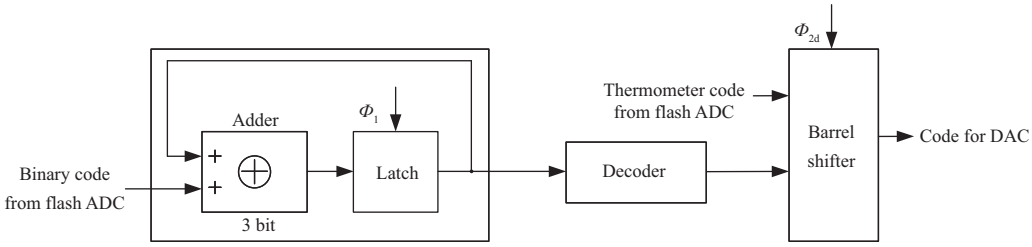
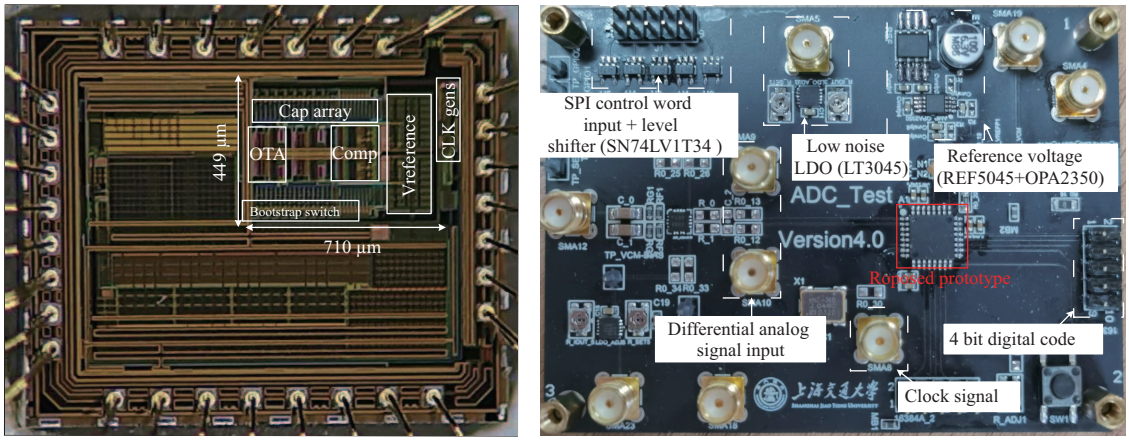
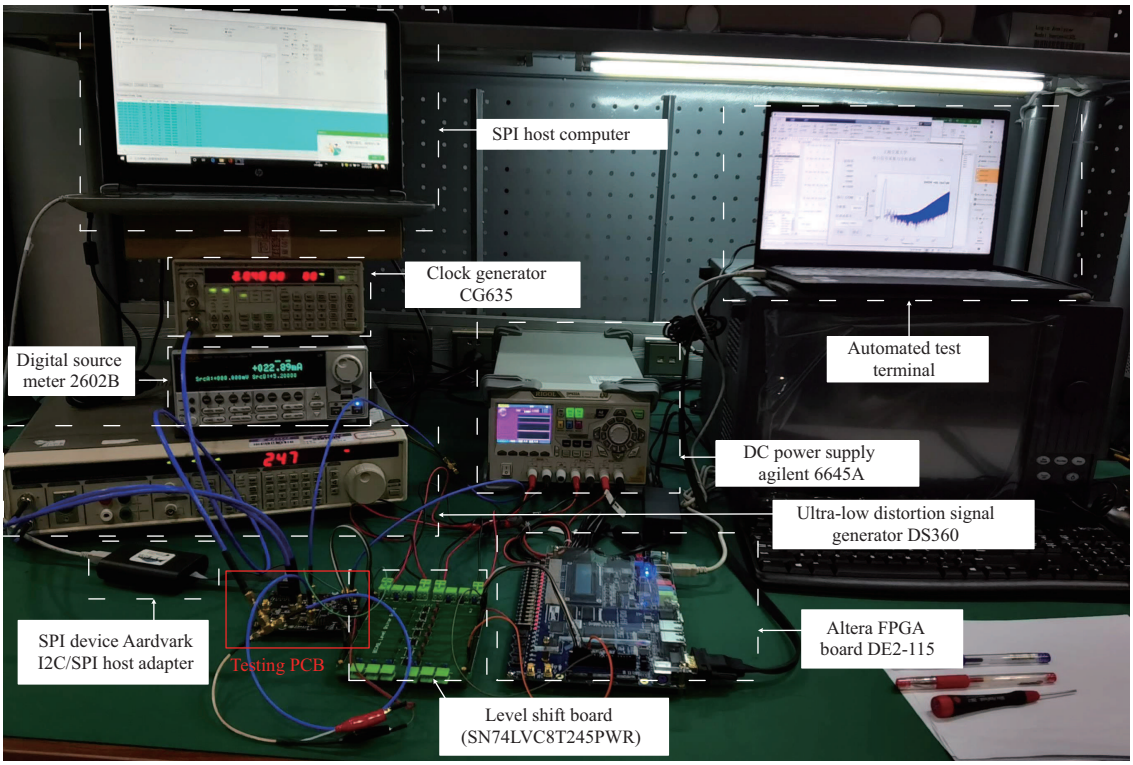


Figure 13 Block diagram of the proposed DWA.



(a) (b)



(c)

Figure 14 (Color online) Measurement setup. (a) Die photograph of the proposed modulator; (b) testing PCB; (c) automated measurement platform.

a 'pointer', which indicates the starting point of the subsentence input data sequence can be formed accordingly. The 'pointer' value is then decoded as 'one-hot-key' and controls the barrel shifter, which consists of an eight-by-eight switch array. In this way, the DAC cells can be selected according to the

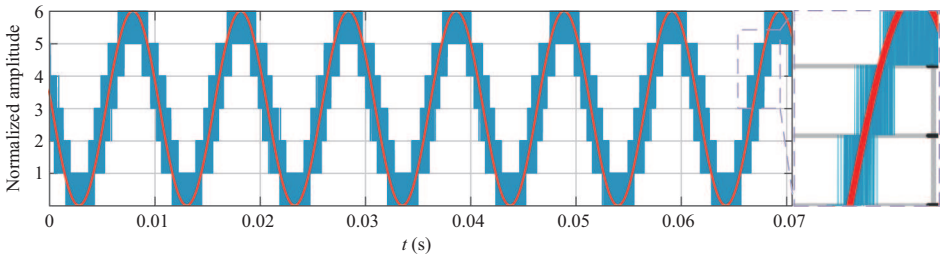


Figure 15 (Color online) Measurement of the reconstructed output with sine-wave input.

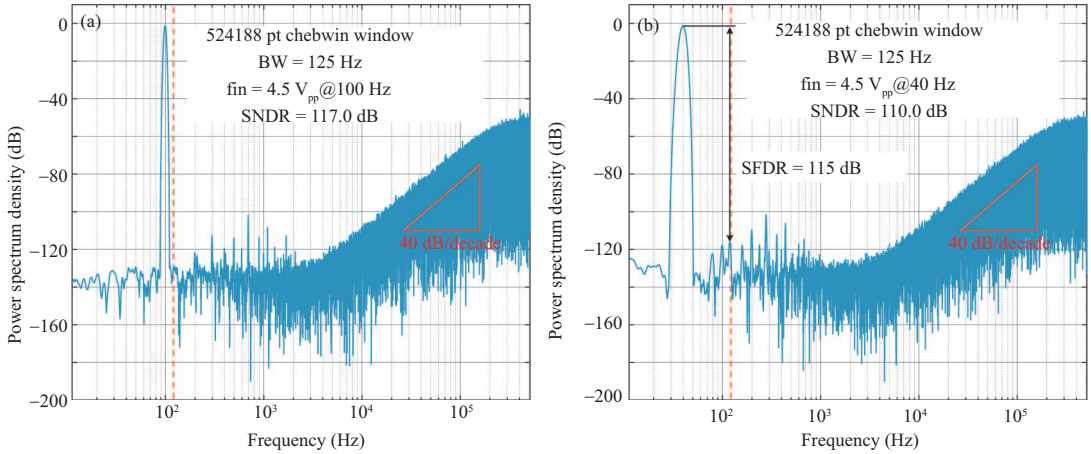


Figure 16 (Color online) Measured 524188-point FFT of the ΣΔ modulator at peak SNDR at 1.024 MS/s (a) fin = 4.5 V_{pp} @100 Hz, BW = 125 Hz; (b) fin = 4.5 V_{pp}@40 Hz, BW = 125 Hz.

subsentence input data sequence and the currently used cells. The output of DAC is feedback to the input of both integrators to close the modulator loop.

4 Experimental results

The prototype has been fabricated with 5 V 180 nm CMOS technology, occupying a core area of 0.32 mm^2 (449 μm×710 μm). Figure 14(a) shows the photograph of the chip. Figure 14(b) and (c) show the validation PCB and the measurement platform, respectively. In our measurement, the analog input signal is generated by the low-frequency high-precision ultra-low distortion signal generator (SRS DS360), whereas the outputs of the ΣΔ modulator are recorded by the FPGA (DE2-115) and subsequently processed by the Matlab (the MathWorks, Inc.) to perform FFT analysis. The power spectrum can be displayed on the host computer in real-time.

Figure 15 shows the measurement of the reconstructed output with sine-wave input. The prototype outputs 4-bit digital codes with pulse-density-modulation (PDM) that include the information of the original input, which can be faithfully recovered through a subsequent decimation filter. Figure 16 shows the measured power spectrum of the modulator with 40 and 100 Hz full-scale analog input, respectively. With 40 Hz input, the measured SNDR and SFDR are 110 and 115 dB within 125 Hz Nyquist bandwidth, respectively. The quantization noise rolls up in 40 dB/decade beyond the Nyquist bandwidth, correspondent to the adopted 2nd-order modulator loop.

Figure 17(a) shows the SNDR versus the input amplitude with/without the CM-ISD. The proposed CM-ISD improves the DR from 99 to 124 dB. The 124 dB dynamic range meets the requirements in most non-invasive EEG acquisition applications. Figure 17(b) shows the total power consumption breakdown of the modulator. The total power consumption is 2.75 mW, dominant by the OTAs, leading to an FoM_S of 170.6 dB. The real 8-channel EEG acquisition has been implemented based on the proposed modulator. Figure 18(a) shows the on-filed measurement setup. In the measurement, the subject wears a multi-channel electrode cap, with the reference electrode on the top of the skull and the bias electrode on the left ear. Figure 18(b) shows the measurement results. When the subject closes the eyes in the rest state, the α-wave can be clearly acquired. The controlling instruction set can be constructed based

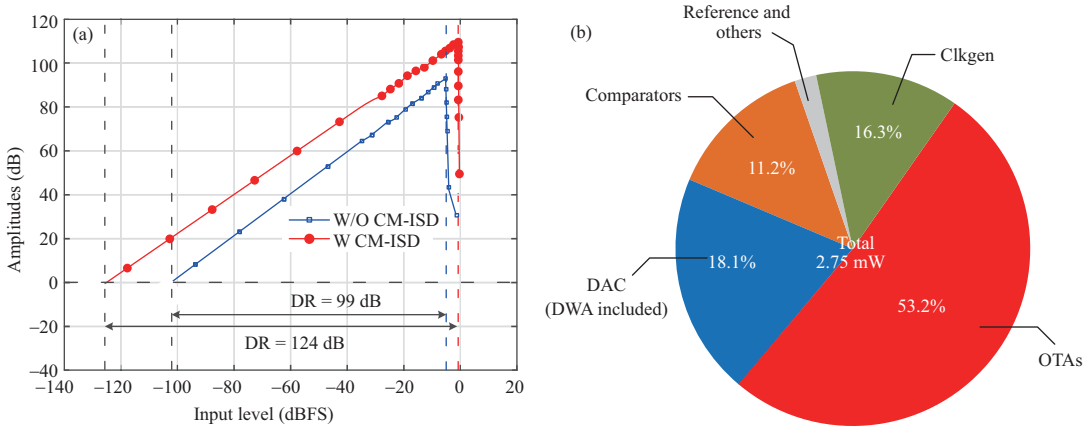


Figure 17 (Color online) (a) Measured SNDR versus input amplitude with/without CM-ISD; (b) total power consumption breakdown among circuit blocks.

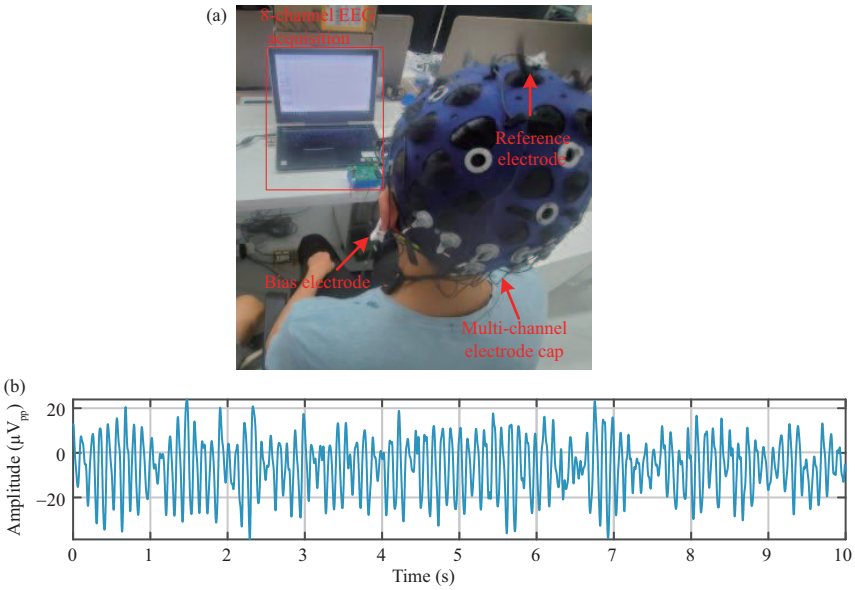


Figure 18 (Color online) (a) On-field EEG measurement platform; (b) measured α-wave with the proposed $\Sigma\Delta$ modulator.

on the acquired EEG with a bandwidth of lower than 100 Hz [35] from the prototype, demonstrating its potential capability to be used in advanced non-invasive BCI systems. Table 2 [36–39][1)] compares the performance to the state-of-the-art study.

Among the listed references, our design achieves the highest DR (124 dB). This is mainly benefiting from the 5 V supply voltage as well as all the aforementioned circuit innovations. It achieves competitive FoM_S (170.6 dB) compared with other studies, particularly among the $\Sigma\Delta$ architectures. As the current consumption of the two OTAs is kept the same for simple layout in our design, the FoM_S could therefore be further improved by cutting down the current of the OTA in the 2nd stage as well as by lowering the supply voltage of the OTAs.

5 Conclusion

In this paper, we propose a DT $\Sigma\Delta$ modulator fabricated with 180 nm CMOS technology, which can be applied to EEG acquisition in a non-invasive BCI. The proposed $\Sigma\Delta$ modulator consumes 550 μA from a 5 V power supply and occupies a core area of 0.32 mm^2. Measurement results show that the proposed

1) Texas Instruments. ADS1299-x Low-Noise, 4-, 6-, 8-Channel, 24-Bit, Analog-to-Digital Converter for EEG and Biopotential Measurements. 2012. https://www.ti.com.cn/tool/zh-cn/ADS1299EEGFE-PDK?keyMatch= tisearch=search-everythingusecase=hardware

Table 2 Performance comparison with state-of-the-art studies

Reference	Architecture	Technology (nm)	Supply voltage (V)	F_s (MHz)	BW (Hz)	SNDR (dB)	DR (dB)	Power (μW)	Chip area (mm^2)	FoM_S[a)] (dB)
JSSC-2006 [36]	IADC	600	5	0.03	7.5	–	120	300	2.08	164
ADS1299-2012	DT $\Sigma\Delta$	–	5	1.024	125–8000	99[b)]	98–119.5[c)]	–	–	–
ISSCC-2015 [37]	DT $\Sigma\Delta$	180	5	0.15	100	100.6	107	505	0.8	160.0
ISSCC-2016 [14]	OS-SAR	55	1.2	1	1000	101	101.7	15.7	0.072	179.7
CICC-2017 [38]	IADC	180	1.5	0.642	1200	96.6	100.2	33.2	0.27	175.8
JSSC-2018 [39]	ZOOM	160	1.8	2	1000	118	120	280	0.25	185.8
TBioCAS-2021 [18]	Hybrid-$\Sigma\Delta$	180	1.8	3.2	100	66.2	108.3	73.8	0.48	169.6
ISSCC-2021 [21]	VCO-based	65	1.2	0.2	1000	92.3	92.3	5.8	0.075	174.7
This work	**DT $\Sigma\Delta$**	**180**	**5**	**1.024**	**125**	**110**	**124**	**2750**	**0.32**	**170.6**

a) $FoM_S = DR + 10 \cdot \log(BW/POWER)$.
b) Including the IA.
c) Including the IA at max gain.

modulator obtains 124 dB DR, 117 dB SNR, and 110 dB SNDR while achieving a competitive FoM_S of 170.6 dB. The real multi-channel EEG measurements demonstrate its potential capability to be applied in advanced non-invasive BCI systems.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant No. 62174109). The authors would like to thank Dongrui GAO, Jiaxin XIE and Shaofei YING in University of Electronic Science and Technology of China for their help and guidance in the real EEG measurements.

References

1 de Salvo B. Brain-inspired technologies: towards chips that think? In: Proceedings of 2018 IEEE International Solid-State Circuits Conference, 2018. 12–18
2 Liu M, Chen H, Chen R, et al. Low-power IC design for a wireless BCI system. In: Proceedings of 2008 IEEE International Symposium on Circuits and Systems, 2008. 1560–1563
3 Hasan M K, Mondal C, Mahmud N A, et al. Performance analysis of SSVEP based wireless brain computer interface for wet and dry electrode. In: Proceedings of 2015 International Conference on Advances in Electrical Engineering (ICAEE), 2015. 64–67
4 Sabor N, Li Y F, Zhang Z, et al. Detection of the interictal epileptic discharges based on wavelet bispectrum interaction and recurrent neural network. Sci China Inf Sci, 2021, 64: 162403
5 Zhao K, Li Y F, Wang G X, et al. A robust QRS detection and accurate R-peak identification algorithm for wearable ECG sensors. Sci China Inf Sci, 2021, 64: 182401
6 Chen W, Chen Y, Chou C, et al. An EEG analog front-end design with wireless communication module for a portable EEG monitoring system. In: Proceedings of 2015 IEEE 5th International Conference on Consumer Electronics, Berlin, 2015. 50–51
7 Burbank D P, Webster J G. Reducing skin potential motion artefact by skin abrasion. In: Proceedings of Medical and Biological Engineering and Computing, 1978. 31–38
8 van Helleputte N, Kim S, Kim H, et al. A 160 μA biopotential acquisition IC with fully integrated IA and motion artifact suppression. IEEE Trans Biomed Circ Syst, 2012, 6: 552–561
9 Dabbaghian A, Kassiri H. An 8-channel 0.45 mm^2/channel EEG recording IC with ADC-free mixed-signal in-channel motion artifact detection and removal. In: Proceedings of 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020. 1–5
10 Ratametha C, Tepwimonpetkun S, Wattanapanitch W. A 2.64-μW 71-dB SNDR discrete-time signal-folding amplifier for reducing ADC's resolution requirement in wearable ECG acquisition systems. IEEE Trans Biomed Circ Syst, 2020, 14: 48–64
11 van Helleputte N, Konijnenburg M, Pettine J, et al. A 345 μW multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction, and integrated DSP. IEEE J Solid-State Circ, 2015, 50: 230–244
12 Wang S H, Hung C C. A 0.3 V 10 bit 3 MS/s SAR ADC with comparator calibration and kickback noise reduction for biomedical applications. IEEE Trans Biomed Circ Syst, 2020, 14: 558–569
13 Yang X, Zhao M, Dong Y, et al. A 14.9 μW analog front-end with capacitively-coupled instrumentation amplifier and 14-bit SAR ADC for epilepsy diagnosis system. In: Proceedings of 2016 IEEE Biomedical Circuits and Systems Conference, 2016. 268–271
14 Shu Y S, Kuo L T, Lo T Y. An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS. In: Proceedings of 2016 IEEE International Solid-State Circuits Conference, 2016. 458–459
15 Lee C, Jeon T, Jang M, et al. A 6.5 μW 10 kHz-BW 80.4 dB-SNDR continuous-time $\Sigma\Delta$ modulator with Gm-input and 300 mV_{pp} linear input range for closed-loop neural recording. In: Proceedings of 2020 IEEE International Solid-State Circuits Conference, 2020. 410–412
16 Bang J S, Jeon H, Je M, et al. 6.5 μW 92.3DB-DR biopotential-recording front-end with 360 mV_{pp} linear input range. In: Proceedings of 2018 IEEE Symposium on VLSI Circuits, 2018. 239–240
17 Jang M H, Lee C, Chae Y. A 134 μW 99.4 dB SNDR audio continuous-time $\Sigma\Delta$ modulator with chopped negative-R and tri-level FIR-DAC. IEEE J Solid-State Circ, 2021, 56: 1761–1771
18 Yang X, Xu J, Ballini M, et al. A 108 dB DR $\Sigma\Delta$-ΣM front-end with 720 mV_{pp} input range and $\pm$300 mV offset removal for multi-parameter biopotential recording. IEEE Trans Biomed Circ Syst, 2021, 15: 199–209
19 Taylor G, Galton I. A mostly-digital variable-rate continuous-time Σ-Δ modulator ADC. IEEE J Solid-State Circ, 2010, 45: 2634–2646

20 He T, Du Y, Jiang Y, et al. A dual-VCO-based quantizer with highly improved linearity and enlarged dynamic range. In: Proceedings of 2011 IEEE 54th International Midwest Symposium on Circuits and Systems, 2011. 1–4

21 Pochet C, Huang J, Mercier P P, et al. A 400 mV_{pp} 92.3 dB-SNDR 1 kHz-BW 2^{nd}-order VCO-based ExG-to-digital front-end using a multiphase gated-inverted ring-oscillator quantizer. In: Proceedings of 2021 IEEE International Solid-State Circuits Conference, 2021. 392–394

22 Huang J, Mercier P P. A distortion-free VCO-based sensor-to-digital front-end achieving 178.9 dB FoM and 128 dB SFDR with a calibration-free differential pulse-code modulation technique. In: Proceedings of 2021 IEEE International Solid-State Circuits Conference, 2021. 386–388

23 Jiang W, Hokhikyan V, Chandrakumar H, et al. A ±50-mV linear-input-range VCO-based neural-recording front-end with digital nonlinearity correction. IEEE J Solid-State Circ, 2017, 52: 173–184

24 Xu J, Nguyen A T, Wu T, et al. A wide dynamic range neural data acquisition system with high-precision Σ-Δ ADC and on-chip EC-PC spike processor. IEEE Trans Biomed Circ Syst, 2020, 14: 425–440

25 Eland E, Karmakar S, Gonen B, et al. A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20-kHz BW. IEEE J Solid-State Circ, 2021, 56: 1207–1215

26 Pavan S, Schreier R, Temes G C. Understanding Delta-Sigma Data Converters. Piscataway: Wiley-IEEE Press, 2017

27 Maloberti F. Data Converters. Berlin: Springer, 2010

28 Candy J C, Temes G C. Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation. Piscataway: Wiley-IEEE Press, 1992

29 Dessouky M, Kaiser A. Very low-voltage digital-audio ΣΔ modulator with 88-dB dynamic range using local switch bootstrapping. IEEE J Solid-State Circ, 2001, 36: 349–355

30 Yoon D Y, Lee H S, Gealow J. Power-efficient amplifier frequency compensation for continuous-time ΣΔ modulators. In: Proceedings of 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), 2013. 562–565

31 Chen F-C, Hsieh C-L. Modeling harmonic distortions caused by nonlinear op-amp DC gain for switched-capacitor sigma-delta modulators. IEEE Trans Circ Syst II, 2009, 56: 694–698

32 Qi L, Sin S W, U S P, et al. A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΔΣ modulator with multirate opamp sharing. IEEE Trans Circ Syst I, 2017, 64: 2641–2654

33 Aghdam E N, Benabes P, Abbasszadeh J. Completely first order and tone free partitioned data weighted averaging technique used in a multibit ΣΔ modulator. In: Proceedings of 2009 European Conference on Circuit Theory and Design, 2009. 53–56

34 Nys O, Henderson R. An analysis of dynamic element matching techniques in sigma-delta modulation. In: Proceedings of 1996 IEEE International Symposium on Circuits and Systems Connecting the World, 1996. 231–234

35 Nayak C S, Anilkumar A C. EEG Normal Waveforms. Treasure Island: StatPearls Publishing, 2021

36 Quiquempoix V, Deval P, Barreto A, et al. A low-power 22-bit incremental ADC. IEEE J Solid-State Circ, 2006, 41: 1562–1571

37 Xu L, Gönen B, Fan Q, et al. A 110 dB SNR ADC with ±30 V input common-mode range and 8 μV offset for current sensing applications. In: Proceedings of 2015 IEEE International Solid-State Circuits Conference, 2015. 1–3

38 Zhang Y, Chen C H, He T, et al. A two-capacitor SAR-assisted multi-step incremental ADC with a single amplifier achieving 96.6 dB SNDR over 1.2 kHz BW. In: Proceedings of 2017 IEEE Custom Integrated Circuits Conference (CICC), 2017. 1–4

39 Karmakar S, Gonen B, Sebastiano F, et al. A 280 μW dynamic zoom ADC with 120 dB DR and 118 dB SNDR in 1 kHz BW. IEEE J Solid-State Circ, 2018, 53: 3497–3507