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Effects of non-fatal electrostatic discharge on the threshold voltage degradation in nano CMOS devices

Hei WONG[1*], Shurong DONG[2] & Zehua CHEN[3]

[1]*Department of Electronic Engineering, City University of Hong Kong, Hong Kong* 999077*, China;*
[2]*Institute of Photonics and Mircroelectronics, Zhejiang University, Hangzhou* 310007*, China;*
[3]*Macronix Microelectronics (Suzhou), Suzhou* 215000*, China*

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Dear editor,

We have conducted experiments by directly applying transmission line pulse (TLP) on MOS devices and revealed that non-fatal electrostatic discharge (ESD) strikes can lead to some long-term reliability issues of the MOS circuits. More interestingly, although gate oxide is considered to be more fragile on an ESD strike and the breakdown voltage of gate oxide is used to define the ESD design window, the non-fatal TLP pulsing on the gate terminal has less effect. Whereas drain TLP strike leads to more pronounced threshold voltage degradation as a result of hot carrier injection near the drain region.

The challenge for ESD protection becomes tougher in the nano CMOS technology because of the chip size limitation and the continued narrowing in the ESD design window (see Figure 1(a)) as specified by the reduced breakdown voltage of the gate oxide and the shrunk operation voltage [1,2]. One important issue that has not been taken sufficient care is the effect of non-fatal ESD strike [2, 3]. When an ESD pulse is less than the breakdown voltage of gate oxide, no action will be taken along with the present ESD design strategies (see Figure 1(a)). By monitoring the stress-induced leakage current of gate oxide struck by a high-speed pulse, it is reported that the non-fatal ESD can still cause degradation of the gate oxide [3].

Results and discussion. The devices used in this investigation are fabricated by a proprietary SOI 65 nm CMOS process with 1.2 nm nitrided gate oxide. TLP strike is done with a Barth 4002 TLP system with a rising time of 10 ns and a pulse width of 100 ns. Figure 1(b) plots typical *I-V* characteristics (left) and compares the effects of gate and drain TLP on the threshold voltage, $V_{\rm T}$ (right). Results suggest that there is threshold TLP voltage, $V_{\rm TLP}$ (gate) $>$ 1 V, and $V_{\rm TLP}$ (drain) $>$ 2 V, to cause notable changes on $V_{\rm T}$. For drain TLP strikes (gate terminal open), the gate oxide charge trapping is similar to the well-known hot-carrier effects [4]. A large drain-to-source voltage ($V_{\rm ds}$) would result in a high field region at the drain side. The electrons in this region can gain sufficient energy to surmount the channel-gate oxide barrier and then localize at the oxide traps. To trigger the impact ionization near the drain, the drain voltage must be large enough. For gate TLP strike, since the gate terminal is isolated with oxide, it allows larger $V_{\rm TLP}$ provides that it does not cause the dielectric breakdown. As shown in Figure 1(b), the gate oxide still functions well for $V_{\rm TLP} < 5$ V. We further conduct multiple TLP strikes. For NMOS, $V_{\rm T}$ shift drops slightly after striking for 10 times and then rises gradually up to 120 times strikes. The initial increase in $V_{\rm T}$ can be considered as electronic trapping and the drop in $V_{\rm T}$ shift afterward should be due to the defects or positive charge generation in the gate oxide. These observations should be due to defect generation as a result of the brokening of the interface or oxide weak bonds [4]. The degradation should reach a saturation value once the weak bonds are fully consumed. For PMOS, the data reported here are taken at a larger $V_{\rm TLP}$ at 5 V to have more significant effects with a reduced number of strikes. Noting that in PMOS the larger $V_{\rm T}$ shift (more negative) indicates a positive charge accumulation or a depopulation of trapped electrons. As the progress of successive TLP strikes, $V_{\rm T}$ shift shows two quasi saturation regions: less than 10 TLP strikes (region I) and larger than 10 strikes (region II). In region I, the $V_{\rm T}$ shift should be due to the net effect of bulk trap electron localization, delocalization, and interface positive charge generation as well. The effect of interface trap generation is partially suppressed by the oxide electron trapping. When the oxide electron traps are mostly filled, the interface trap generation dominates which leads to the further increase (more negative) in $V_{\rm T}$ shift. Since the amount of weak interface bonds at the interface is limited, the interface trap generation will slow down which yields the second saturation region. These characteristics agree with the hot-carrier trapping and charge generation model proposed earlier [4]. Figure 1(d) summarizes the possible mechanisms taken place with drain and gate non-fatal TLP strike for NMOS and PMOS. For drain TLP, the high-speed pulse would induce impact ionization in the high-field region of reversely-biased

* Corresponding author (email: heiwong@ieee.org)

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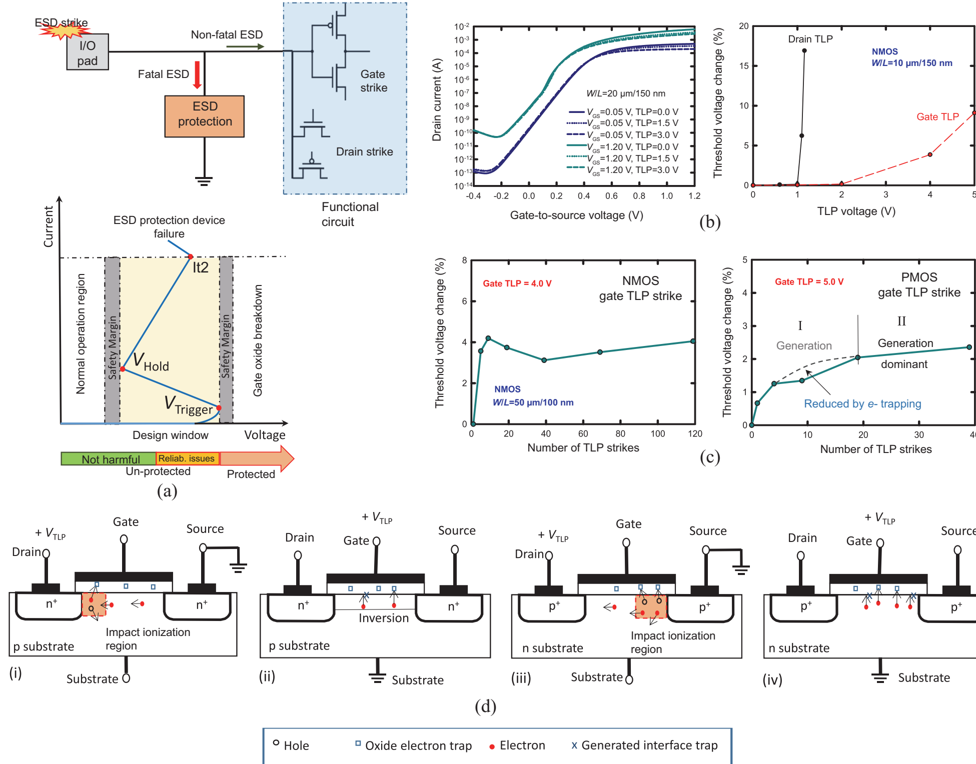

Figure 1 (Color online) (a) Illustration of the idea for ESD protection and the possible consequences of non-fatal ESD strikes on a CMOS circuit. Large ESD pulses that are close to the breakdown voltage of the gate oxide have been considered in ESD protection design whereas no action has been taken for small ESD pulses that can strike on a CMOS circuit and may give rise to some reliability issues. (b) Typical *I*-*V* characteristics under gate TLP strikes (left) and comparison of the effects of drain and gate TLP on the threshold voltage degradation (right). (c) Multiple non-fatal gate TLP strikes on threshold voltage variation for both NMOS and PMOS. (d) Illustration of the mechanisms leading to threshold voltage changes for different TLP strikes: (d-i) drain TLP on NMOS with channel hot electron injection; (d-ii) gate TLP on NMOS with channel electron injection; (d-iii) drain TLP on PMOS with substrate hot electron injection; (d-iv) gate TLP on PMOS with substrate electron injection.

drain or source junction (see Figures 1(d-i) and (d-iii)). For gate TLP, the threshold voltage shift is much smaller although the pulse levels are much higher. These observations are attributed to the depopulation of trapped oxide charge under positive gate pulse (see Figures 1(d-ii) and (d-iv)). Non-fatal ESD strike, hot-carrier stressing and total ionizing dose irradiation effects [5, 6] share some similar physics and device performance degradation issues with certain deviations. They are good complement studies to one other.

Conclusion. By applying non-fatal ESD strikes directly on the drain or gate terminal of MOS transistors, we found that a low-voltage drain TLP strike can cause significant channel hot-carrier injection into the gate oxide and give rise a large threshold voltage shift. Although gate oxide is more fragile and has been the key target for ESD protection, a large non-fatal ESD pulse caused less effect on V_T degradation than the drain ESD strike. The gate TLP strike can still cause interface trap generation and gate oxide electronic trapping. From the system point of view, our results indicate that the drain ESD strike above a certain threshold could cause the soft failure of the digital circuit because of the significant change in threshold voltage. Hence direct connecting source or drain to I/O pad should be avoided otherwise additional ESD protection circuit should be introduced for protecting the drain terminal. Gate terminal is more robust against non-fatal ESD strike but it still causes long-term instability because the ESD strike can cause interface trap generation. It is worth a further detailed investigation on the effects of non-fatal ESD strike CMOS circuits. Further theoretical modeling or quantitative correlation of the degradation characteristics with the non-fatal strike parameters will lead to a better understanding of the underlying physics and benefit the circuit design aspect.

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