SCIENCE CHINA
Information Sciences

• LETTER •

February 2022, Vol. 65 129402:1–129402:2
https://doi.org/10.1007/s11432-020-3169-x

SEU sensitivity and large spacing TMR efficiency of Kintex-7 and Virtex-7 FPGAs

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Received 17 August 2020/Revised 10 November 2020/Accepted 17 January 2021/Published online 24 May 2021

Citation Cai C, Ning B X, Fan X, et al. SEU sensitivity and large spacing TMR efficiency of Kintex-7 and Virtex-7 FPGAs. Sci China Inf Sci, 2022, 65(2): 129402, https://doi.org/10.1007/s11432-020-3169-x

Dear editor,

The static random-access memory (SRAM)-based field programmable gate arrays (FPGAs) mainly composed of extensive configurable logic blocks (CLBs), high-speed embedded memories (BRAMs), and a set of programmable routing, wires or switch boxes [1, 2] are commonly used in avionic and space fields as its advanced performance and high flexible in-field reprogramming abilities [2]. However, the advanced SRAM-based FPGAs are susceptible to radiation effects, especially for the single event upsets (SEUs) [3–5]. If an SEU occurs in a configuration memory (CRAM), the configuration of routing connections, or the configuration of look-up tables (LUTs) and D flip-flops (DFFs) may change to cause malfunction [5, 6]. Hence, the testing methodology, the influence of SEU, and the fault mitigation strategies are necessary for SRAM-based FPGAs to promote the space application. This study evaluates the SEU sensitivities and analyzes the potential space applications of the high-performance Kintex-7 (XC7K325T) and Virtex-7 (XC7VX690T) FPGAs. Full SEU characterization of the advanced FPGAs is provided by using diverse testing modes under a series of heavy-ion irradiations. The convincible on-orbit rates for different applications of FPGAs are predicted to evaluate the practical application value in space missions.

Experimental setup. Four test modes including the bitstream test, BRAM test, and DFF triple module redundancy (TMR) test are employed for heavy ion irradiation experiments. All the BRAM and CRAM resources in FPGAs are characterized in bitstream test, by comparing the read-back bitstreams which is suitable to show the static SEU sensitivity and provide basic SEU results for the FPGAs. An application-oriented trial for BRAM test is implemented by instantiating BRAM module of FPGAs as an actual memory with address data pattern. Besides, the configured DFFs are valuable to analyze the SEU sensitivity of the logical resources, and the TMR test employs three radiation hardened DFFs labeled as DFF1, DFF2 and DFF3 to characterize the effectiveness of the TMR hardening techniques for the 28 nm FPGA. DFF1 including an asynchronous reset is a standard DFF chain without hardening, and only for the DFF1, the consecutive DFF stages are constrained into two consecutive slices; both DFF2 and DFF3 use TMR strategy with two additional chains for redundancy, while only DFF3 employs three separated clock buffers. Another important thing is that plenty of high-energy heavy ions with changeable linear energy transfer (LET) ranges are used in irradiation tests, which are essential in full characterization of the SEU sensitivities and accurate prediction of the on-orbit rates of FPGAs.

Irradiation results. The SEU cross sections for CRAMs and BRAMs are collected and classified, and the results for XC7K325T and XC7VX690T FPGAs are shown in Figure S1(a) and (b), respectively. For these two FPGAs, the SEU thresholds are both below 2.4 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}. In the bitstream test, the cross sections of CRAMs are slightly higher than the cross sections of BRAMs. While the BRAM is SEU sensitive for instantiation test with address data pattern. The high SEU cross section is mainly due to the additional interconnecting resources utilized in BRAM instantiation test. The SEUs existed in the interconnecting resources may affect the function of BRAMs, leading to a substantial increment of SEU cross sections. The static mode is employed in DFF (TMR) test, and a rational scrubbing frequency is required during the test in case of the accumulation of error bits. The error counts versus time under high-LET and low-LET ions irradiation are shown in Figure S1(c) and (d), respectively. Not limited to the bit cell upset but all kinds of errors are counted, and the results of the SEU cross sections are shown in Figure S1(e). The SEU thresholds for DFF2 and DFF3 are improved. Comparing

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the SEU results of DFF2 and DFF3, it is found that the SEU tolerance of DFF3 is low, which is due to the additional clock buffers in DFF3. Therefore, as for the hardened chains, the increase of SEU cross section induced by the additional occupation of radiation-sensitive buffer is not negligible. The multiple bit upsets (MBUs) and burst errors under the normal function of DFFs are distinguished. None of the MBU and burst error occurs in DFF2 and DFF3 (the functional failures are not included), as presented in Figure S1(f). Besides, the burst error increases significantly in high LET, and the MBU merely appears in ^{209}Bi irradiation with LET value at 49.9 MeV $\cdot$ cm^2 $\cdot$ mg^{-1}, and the cross sections of MBU are $\sim$ 2 orders of magnitude lower than the single bit upset.

On-orbit prediction. The on-orbit event rate is an essential parameter for the operation security of the aircraft or spacecraft systems. According to our systematic SEU evaluation of heavy ions, the on-orbit event rate prediction can be achieved convincingly. The event rate prediction based on the on-orbit LET spectrum and measured SEU cross sections is performed with the CREME96 software [7], as shown in Figure S1(g) and (h). All kinds of upsets are counted in the SEU prediction of DFFs, leading the event rate increased significantly when compared with the mere cell upsets. As for the users, it is necessary to employ hardening strategies to satisfy the event rate criteria of missions and maximize the performance of the devices. In addition, widening cell spacing is implemented based on a specially compiled constrain file without extra area and resource penalty. Benefiting from the widening cell spacing, the effectiveness of TMR structure is observed. The hardened DFFs may be acceptable in space, which is related to the actual environment and mission requirements. The application-oriented BRAM test presents orders of magnitude higher in event rate, which verifies that an accurate SEU prediction should according to the actual application conditions in case of the overestimation of the radiation tolerance. Thus, the accurate predictions of on-orbit event rate are helpful for researchers to determine whether the devices can be applied in space missions and what kinds of error mitigation strategies are required.

Conclusion. This study presents the impact of heavy ions on the SEU features and predicts the on-orbit SEU rate for the space application of high-performance 28 nm bulk SRAM-based FPGAs. The measured SEU cross sections are employed to characterize the radiation sensitivities. The results show a significant difference among the SEU cross sections of CRAMs, BRAMs, and DFFs. The employed test methods have an influence on SEU cross section results, which is verified in our application-oriented BRAM test. In addition, the radiation-sensitive resource such as the clock buffers is essential to further improve the radiation tolerance of FPGA. These results indicate that the reasonable hardening strategies are still useful for the 28 nm bulk CMOS high-performance FPGAs, which significantly promote the space application of the 28 nm high- performance FPGAs.

Acknowledgements The work was jointly supported by National Natural Science Foundation of China (Grant No. 11690041), State Key Laboratory of ASIC & System (Grant No. 2020KF009), and HIRFL (Grant No. JIZR20GY002).

Supporting information Figure S1. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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