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Stateful implication logic based on perpendicular magnetic tunnel junctions

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Abstract As the conventional von Neumann architecture meets critical limitations of data transfer bandwidth and energy consumption, perpendicular magnetic anisotropy magnetic tunnel junction based processing-in-memory paradigm attracts extensive attention as a promising substitute thanks to its non-volatility, low-power switching, fast access and infinite endurance. In this work, we propose and experimentally demonstrate a new spintronic implication logic gate that consists of two parallel perpendicular magnetic anisotropy magnetic tunnel junctions with different diameters. Material implication and furthermore NAND logic functions are implemented by all electrically-controlled operations. The reliability of this structure is verified, especially in sub-20 nm node, which shows great potential for large-density processing-in-memory applications.

Keywords perpendicular magnetic anisotropy magnetic tunnel junction, implication, spin transfer torque, spintronic implication logic gate, processing-in-memory

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1 Introduction

In digital electronics, Shannon proved that AND, OR, and NOT can be considered as three basic Boolean logics to compute the results of any compound Boolean logic [1]. Based on this fundamental logic group, digital logic has achieved a remarkable development. However, the choice of basic logic group is not unique. Another special logic operation is "material implication" (IMP). With the combination of FALSE, whose value is always 0, IMP can also act as a complete basis for Boolean logic and could provide a more flexible alternative for complex circuit design [2].

At present, data transfer bandwidth and energy consumption are two critical limitations of conventional von Neumann architecture due to the separation and the performance mismatch of processor and memory units [3,4]. Processing-in-memory (PIM), combining logic and storage on a same die, can reduce the latency and improve the data transfer rate, which is expected to overcome the speed and energy bottlenecks [5–8]. Furthermore, the adoption of fast non-volatile electronic devices in PIM architecture provides more configurable resources and lower power consumption [9–11]. Among them, the perpendicular magnetic anisotropy magnetic tunnel junction (p-MTJ), which consists of two perpendicular magnetic layers (free layer and reference layer) separated by a thin insulating layer as shown in Figure 1(a), is becoming one of the most promising computing units due to its non-volatility, low-power switching, fast access and infinite endurance [12–18]. Besides, using spin-transfer torque (STT) carried by a current to switch the state improves the compatibility of p-MTJ with CMOS technology [19–22]. Thanks to these advantages, several interesting designs of p-MTJ based IMP logic gate have been proposed, showing great

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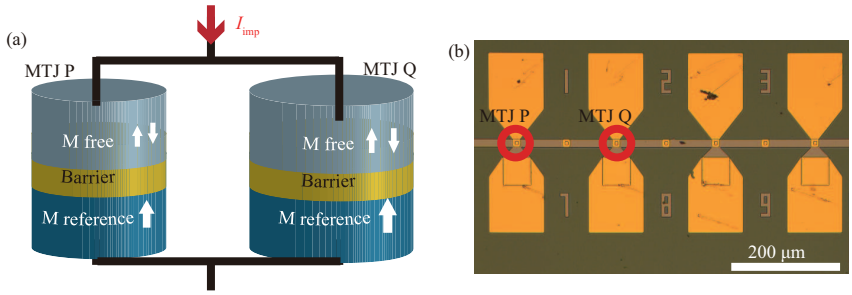


Figure 1 (Color online) (a) Layout of SILG. MTI P and MTJ Q are connected in parallel. (b) Top view of the fabricated SILG devices by optical microscope. Two MTJs named P and Q with different diameter are selected to form an SILG.

advantages compared to the conventional computing architecture [23, 24]. However, an additional magnetic field [13, 14, 23] or resistor [10, 24] is necessary to complete their operations, which will significantly influence their energy efficiency and scalability.

In this paper, we first introduce a new design of spintronic implication logic gate (SILG) consisting of two parallel p-MTJs without additional resistors. According to this design, p-MTJ based SILG are fabricated and characterized at room temperature. Afterward, IMP and furthermore NAND logic functions are performed by all current-driven operations. Finally, the reliability of IMP operations in the SILG device is verified, showing a promising way to realize the PIM architecture with low power consumption, a high operation speed, and large scalability.

2 SILG design and fabrication

The SILG proposed in this paper contains two parallel p-MTJs, P and Q, which have different diameters as shown in Figure 1(a). Different from the structure of the previously reported IMP stateful logic gates [2, 10], we use the freedom of size modulation of p-MTJs to realize IMP logic functions instead of an additional resistor which may lead to low scalability and a complex fabrication process. A constant current pulse ($I_{\rm imp}$) is applied to the SILG as a clocking signal during logic operations. An MTJ usually has two states corresponding to logic value 0 and 1. Here, we define the parallel magnetization (PM) of MTJs which leads to a low-resistance state as logic value 1, and the antiparallel magnetization (APM) which results in a high-resistance state as logic value 0. The state of MTJ P and Q represent the logic variables p and q, respectively, which are the inputs of SILG. The output, named as q', is the state of MTJ Q after applying $I_{\rm imp}$.

Starting from the bottom, the starks consisting of Ta(5)/Ru(30)/Ta(0.7)/Pt(1.5)/6 × [Co(0.5)/Pt(0.2)]/Co(0.6)/Ru(0.8)/Co(0.6)/3 × [Pt(0.2)/Co(0.5)]/W(0.25)/CoFeB(1.0)/MgO(0.8)/CoFeB(1.3)/W(0.3)/CoFeB(0.5)/MgO(0.75)/Pt(0.4)/Ta(3)/Ru(8) (nominal thickness in nm) are deposited on thermally oxidized Si substrate by DC/RF magnetron sputtering and patterned into pillars by electron lithography and Ar ion milling. As shown in Figure 1(b), two p-MTJ pillars named P and Q, of which design diameter are 50 and 60 nm, respectively, form an SILG. They have individual top electrodes and a shared bottom electrode. This structure can support the characterization of each single MTJ as well as logic implementations in two MTJs. It is worth noting that the resistance of metal electrodes is two orders smaller than that of MTJs. Therefore, all the resistance measurements of MTJs are performed by the two-probe method.

Magnetic field and current sweeps are first performed at room temperature to characterize the magnetoresistance and STT behavior in each nanopillar of the SILG. Figure 2(a) shows the individual resistance transitions of two MTJs induced by out-of-plane magnetic field. A positive perpendicular magnetic field leads to a PM state and therefore a low resistance, while a negative field causes a reverse state. The tunneling magnetoresistance ratio (TMR) is larger than 90%. It should be noted that there is a stray field caused by incomplete etching of pinned layers and therefore all the followed electrical measurements are performed under an external perpendicular field (−400 Oe) to offset the influence of the stray field. This stray field could be eliminated by improving the etching process.

Figure 2(b) presents the individual STT switching measured by sweeping voltage pulses with a duration (τ) of 1 ms. It is obvious that the threshold voltage of MTJ Q is smaller than that of MTJ P. The difference comes from the size dependence of the effective perpendicular magnetic anisotropy field ($H_{\rm eff}$) [25]. As the

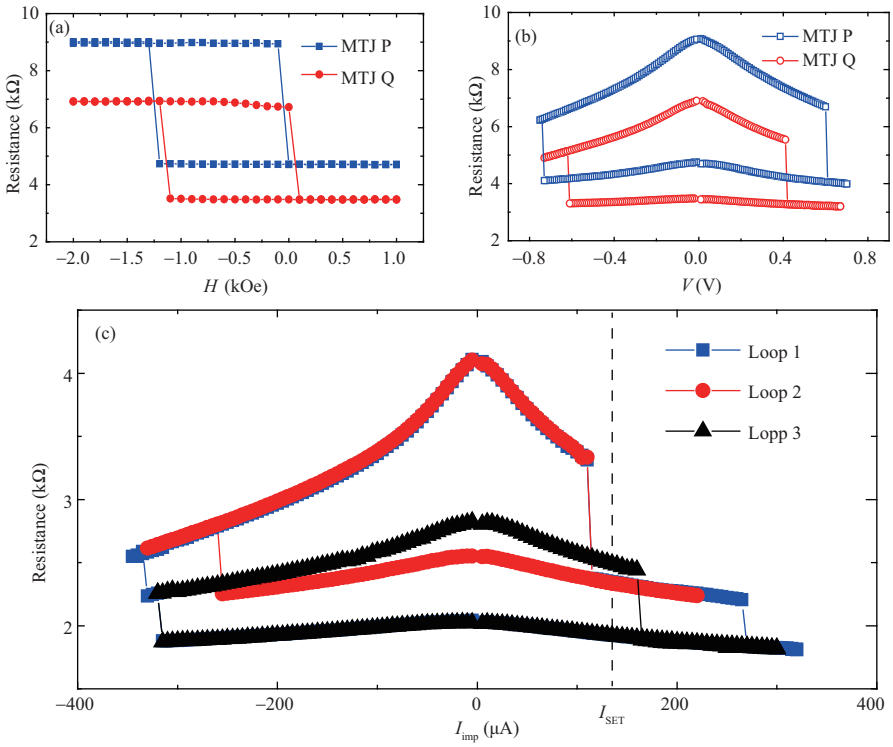


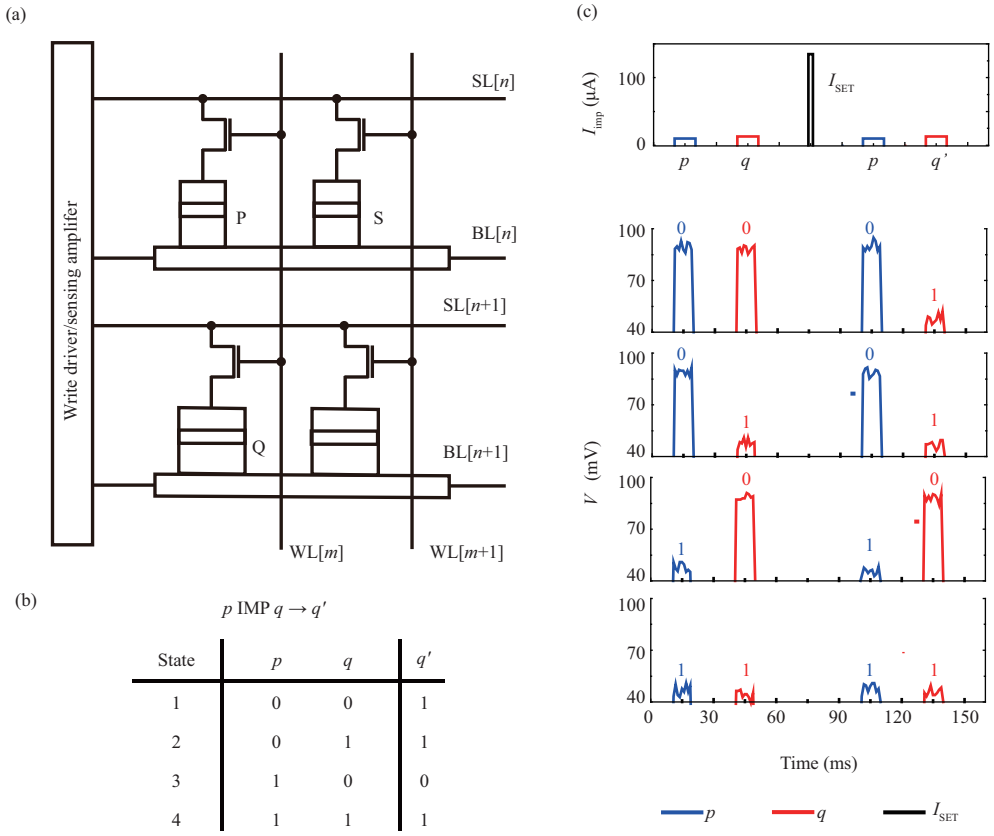
Figure 2 (Color online) (a) Individual magnetoresistance as a function of out-of-plane magnetic field. (b) Individual STT switching measured by voltage pulses with a duration (τ) of 1 ms. (c) STT switching of SILG. Two MTJs are connected parallelly. Loop 1 shows that two MTJs are switched successively by sweeping current pulses. Loops 2 and 3 present the STT switching of MTJ Q with MTJ P in APM and PM state, respectively. An external perpendicular magnetic field (−400 Oe) is applied to reduce the influence of stray field.

diameter of an MTJ shrinks, the demagnetization factor along out-of-plane (in-plane) direction decreases (increases), causing a smaller demagnetization field and therefore a larger $H_{\rm eff}$ [25]. Another possible reason is the edge enhancement of perpendicular magnetic anisotropy (PMA). A larger perimeter-area ratio results in a stronger PMA [26]. To determine the suitable value of $I_{\rm imp}$, the current dependent resistance state of SILG is measured by sweeping $I_{\rm imp}$ as shown in Figure 2(c). Loop 1 shows that MTJ Q and P are switched successively. Compared with MTJ P, MTJ Q can be switched with smaller $I_{\rm imp}$, corresponding with the result of Figure 2(b). The key point is that the threshold current of MTJ Q from APM to PM state is 110 μA with MTJ P in APM state while it changes to be 160 μA with MTJ P in PM state as shown in Loops 2 and 3. It means that the state of MTJ P will determine whether MTJ Q switches when $I_{\rm imp}$ is set between 110 and 160 μA. In other words, the output of SILG, q', depends on the input q as well as p. To reduce the influence of stochastic switching, $I_{\rm imp}$ is chosen as 135 μA.

The above measurements are performed by a Keithley 6221 current source and a Keithley 2182 nanovoltmeter. The applied pulse width is chosen as 1 ms which is far from the switching speed under precessional reversal mode. To verify the speed and power-efficiency performance of MTJs for PIM applications, we perform the ultrafast switching measurement as shown in Figure A1 of Appendix A. The magnetization can be switched within 3 ns and the power consumption can be as low as 4.5 pJ as shown in Table B1 of Appendix B, showing the great potential of MRAM for PIM applications. Since the implementation of IMP logic function in our devices needs a constant current ($I_{\rm imp}$), the current source Keithley 6221 rather than the arbitrary waveform generator is used in the following PIM function demonstrations.

3 Illustration of IMP and NAND operations in SILG

The leakage current of p-MTJs can be over 100 μA, which cannot be directly applied for logic operations. To realize PIM architecture, the 1 T (transistor) — 1 MTJ, the typical magnetic random access memory (MRAM) unit structure, is adopted as shown in Figure 3(a). The transistor can not only play the role of



State	p	q	q'
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

Figure 3 (Color online) (a) Design of SILG in 1T-1MTJ STT-MRAM structure. (b) The truth table of IMP logic. (c) Illustration of the IMP operations performed by the fabricated SILG device. The pulse width of the set current is 1 ms and the resistance state is read out by repeating ten times.

a selector, but also eliminate the impacts of the leakage current. Moreover, the TMR ratio of p-MTJs is about 90% which will affect the read operations. Hence, a sensing circuit is applied to amplify the readout signal [27]. It should be noted that MTJs of the same size should share the same bit line (BL) to simplify the peripheral circuit. During logic operations, the inputs of SILG can be initialized by the memory write operations. And then the clocking signal $I_{\rm imp}$ can be applied by turning on two corresponding transistors at the same time. In the end, the output can be read out by memory read operations.

Material implication, i.e., p IMP q, means "if p, then q". To verify the IMP logic function, the four states in Figure 3(b) have to be achieved. The critical point for the operations of SILG is to choose an appropriate $I_{\rm imp}$ that could motivate MTJ Q from APM to PM in state 1 while keep MTJ Q unchanged in state 3. By referring to the Loops 2 and 3 of Figure 2(c), $I_{\rm imp}$ is determined as $I_{\rm SET} = 135$ μA. In the demonstration of IMP logic functions, two MTJs are first initialized separately according to the result shown in Figure 2(b). Before and after applying $I_{\rm SET}$, the resistance of MTJ P and Q are measured successively by small current pulses to characterize the inputs p, q and output q' of SILG as shown in Figure 3(c). To simplify the sensing amplifier, we use 10 μA to measure the resistance of MTJ P and 13 μA to characterize that of MTJ Q. Here, the current is generated by Keithley 6221 current source and the voltage is measured by a Keithley 2182 nanovoltmeter. The measurements are repeated 10 times. The measured voltage larger (smaller) than 70 mV presents APM (PM) state and logic value 0 (1). The output of IMP logic functions shown in Figure 3(c) is consistent with the truth table shown in Figure 3(b).

To perform NAND logic functions by using the SILG, three steps are needed as shown in Figure 4(a). We add another MTJ named S which has the same size as MTJ P and stores logic variable s. The inputs of NAND logic, p and s, are stored in MTJ P and S. MTJ Q is first individually initialized to APM state by applying a current $I_{\rm CLEAR} = -180$ μA. Afterwards, the IMP logic operations between MTJ S and Q are executed as shown in Figure 4(b). The output value q' stored in MTJ Q is characterized. Moreover, the same logic operations are completed between MTJ P and Q by changing the state of corresponding transistors. $I_{\rm imp}$ of these two cycles of IMP logic operation keeps the same. The final output q'' of NAND

(a) p NAND $s \rightarrow q''$

Step	Operation	Action objects	Clocking signal
1	$q = 0$	MTJ Q	$I_{imp} = I_{CLEAR}$
2	s IMP $q \rightarrow q'$	MTJ S and Q	$I_{imp} = I_{SET}$
3	p IMP $q' \rightarrow q''$	MTJ P and Q	$I_{imp} = I_{SET}$

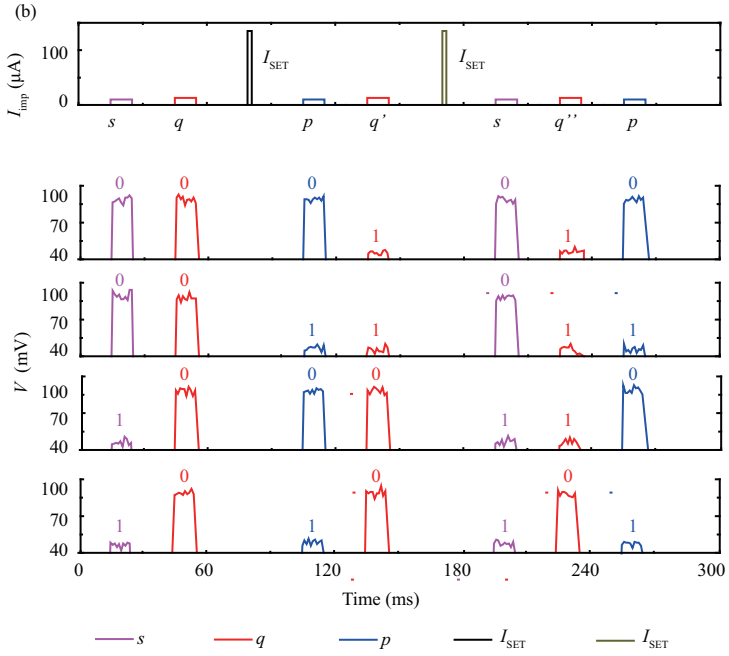


Figure 4 (Color online) (a) Steps to realize NAND logic functions using IMP logic. (b) Illustration of NAND operations implemented by the SILG device. The pulse width of the set current is 1 ms and the resistance state is read out by counting ten times.

logic is stored in MTJ Q. The result shown in Figure 4(b) is consistent with NAND logic functions.

4 Reliability of IMP operation in SILG

P-MTJs have a different probability of switching depending on the applied current, which can significantly influence the performance of SILG. To test its reliability, the switching probability is measured as shown in Figure 5(a). Each point indicates the probability of switching which is measured by 100 repetitive cycles with a given current ($\tau = 1$ μs). Moreover, the lines in Figure 5(a) illustrate the fitting results based on the theoretical expression of p-MTJ switching probability which is expressed as

$$P = 1 - \exp\left\{-\frac{\tau}{\tau_0}\exp\left[-\Delta_0\left(1 - \frac{J}{J_{C0}}\right)\right]\right\}, \tag{1}$$

where τ_0 is the inverse of attempt frequency, Δ_0 is the thermal stability, J is the density of the applied current and J_{C0} is the intrinsic threshold current density [28]. Compared to MTJ P, MTJ Q has a smaller J_{C0}, which is caused by its larger size.

To determine the reliability of IMP operations, it is necessary to analyze the probability of each state shown in the truth table. For state 1, only when MTJ Q is switched and MTJ P remains unchanged, the operation succeeds. Therefore, the error rate of this state can be expressed $P^1_{ER} = 1 - P^1_Q(1 - P^1_P)$, where P^1_Q is the switching probability of MTJ Q from APM to PM when MTJ P is in APM, and P^1_P is the switching probability of MTJ P from APM to PM with MTJ Q in APM. As shown in the top panel of Figure 5(b), the TMR of MTJs has no obvious influence on P^1_{ER} as it only depends on the difference of

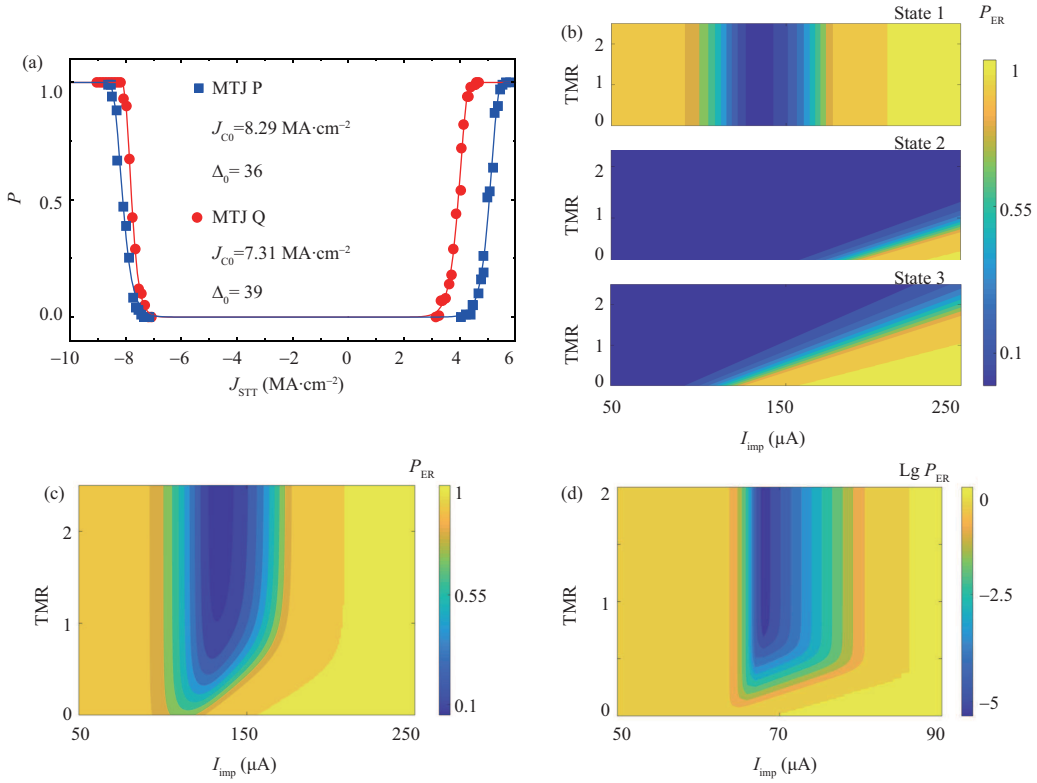


Figure 5 (Color online) (a) Switching probability of P and Q along with STT current density. The discrete points are experimental results and the lines are fitting results according to Eq. (1). (b) $P_{\rm ER}$ of each state calculated with MATLAB. Error rate of state 4 is 0. (c) $P_{\rm ER}$ of our fabricated SILG calculated with MATLAB according to Eq. (2). (d) $P_{\rm ER}$ of the SILG based on the present advanced MTJs whose diameters are 10 and 15 nm, respectively [29].

the intrinsic threshold voltage (or intrinsic current density). For state 2, the error rate $P^2_{\rm ER} = P^2_{\rm P}$, where $P^2_{\rm P}$ is the switching probability of MTJ P with MTJ Q in P state. As MTJ Q is already in PM state, the switching of MTJ P is more difficult as shown in the middle panel of Figure 5(b). For state 3, the error rate $P^3_{\rm ER} = P^3_{\rm Q}$, where $P^3_{\rm Q}$ is the switching probability of MTJ Q with MTJ P in PM state as shown in the bottom panel of Figure 5(b). In this state, a higher TMR will lead to a lower $P^3_{\rm ER}$. For state 4, $I_{\rm imp}$ will not change their state because these two p-MTJs are already in PM state. As a result, the error rate of this state $P^4_{\rm ER} = 0$. In conclusion, the error rate of SILG is expressed as

$$P_{\rm ER} = 1 - P^1_{\rm Q}(1 - P^1_{\rm P}) + P^2_{\rm P} + P^3_{\rm Q}. \tag{2}$$

Accordingly, $P_{\rm ER}$ is calculated as shown in Figure 5(c). The main limitation of reliability comes from $P^1_{\rm ER}$ which is determined by the size difference between two MTJs. With an appropriate $I_{\rm imp}$, $P_{\rm ER}$ of our fabricated SILG can be controlled under 6% with the limited size difference (only 10 nm). A larger size difference between two MTJs can contribute to a larger difference of intrinsic threshold current density and therefore better reliability.

Furthermore, using shape anisotropy based MTJs with smaller sizes can improve the reliability of SILG. We calculate the error rate of our SILG design based on the shape anisotropy p-MTJs whose diameters can be as small as 10 and 15 nm, Δ_0 can be as large as 80 and 60, J can be 32 and 25 MA·cm^{-2}, respectively [29]. The error rate of this SILG can be lower than 10^{-5} as shown in Figure 5(d). In terms of fabrication variations, the high reliability can be realized by shrinking the size and increasing the size difference since the shape anisotropy based MTJs of smaller size have larger $J_{\rm C0}$ as well as Δ_0 [29].

5 Conclusion

We propose a new design of SILG, consisting of two parallel MTJs without additional memristors, which can simplify the structure as well as fabrication process. A writing speed of 3 ns and a power consumption of 4.5 pJ/bit in the MTJs are experimentally demonstrated to show the great potential of MRAM for PIM

applications. The stateful IMP logic operations and further NAND logic functions are implemented with our SILG devices. The error rate of IMP logic operations executed by the fabricated SILG device can be lower than 6%. Especially, using shape anisotropy MTJs with sub-20 nm node could reduce the error rate down to 10^{-5}. This work experimentally proves the feasibility of all electrically-controlled SILG, which could provide an alternative way for efficiently realizing complex logic functions and promote the development of large-density PIM applications.

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Supporting information Appendixes A and B. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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