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Implication Logic Based on Perpendicular Magnetic Tunnel Junctions

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Appendix A Ultrafast switching measurements of p-MTJs

We perform the maximum speed and the power consumption measurements of the MTJs we used for IMP logic gates as shown in Fig. A1. An arbitrary waveform generator (AWG) with the sampling rate of 5GHz is used to generator a 10 ns pulse with a rise time about 100ps and a high band-width oscilloscope (4GHz) is integrated to measure the dynamic signal of MTJs as shown in Figure A1(a). It should be noted that the Coplanar Waveguide (CPW) is used in our device to measure the ultra-fast switching of MTJs as shown in Figure A1(b). The diameter of this MTJ is 60 nm, the same as MTJ Q presented in the manuscript.The magnetization can be switched by STT in 3 ns as shown in Figure A1(c) and Figure A1(d).

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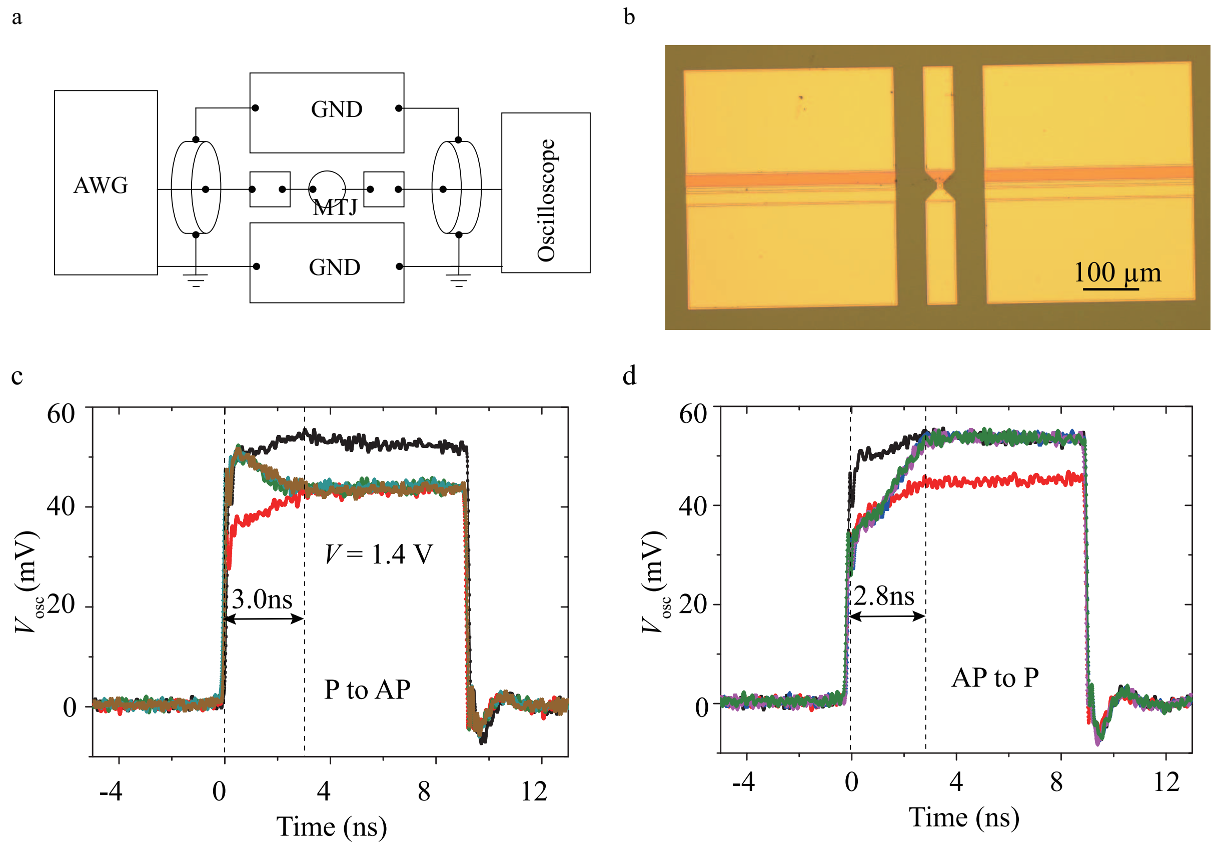

Figure A1 Ultrafast switching measurements. (a)Setup of ultrafast switching measurement. (b)Top view image of an MTJ with CPW design. The dynamic signal of magnetization switching from parallel (P) to anti-parallel (AP) states (c) and from AP to P states (d). It should be noted that the black curve presents the signal of P sate and the red one shows the signal of AP state. The curves of other colors are the dynamic signals of magnetization switching, where the 3ns switching time parameter is read out.

Appendix B Performance metrics of nonvolatile-device based IMP logics

The performance comparison between MRAM and RRAM for IMP logic functions is listed in the Table B1. The speed and the power consumption comparisons show great potential of MTJs for IMP logic applications. Besides, the size of MTJs is comparable with that of memristors. More importantly, the resistances of parallel and antiparallel states are more reproducible.

Table B1 Performance metrics of nonvolatile-device based IMP logics

Memory	Speed (ns)	Power consumption (pJ/bit)	size	reproducibility
MRAM (This work)	3	≈ 4.5	50 nm x 50 nm and 60 nm x 60 nm	high
RRAM [1]	2000	$\approx 1.5 \times 10^4$	Two junctions of 50 nm x50 nm and a long nanowire as a resistor	low
RRAM [2]	10^6	$\approx 10\,(set)\; and \approx 10^7\,(reset)$	5 μm x5 μm	low

References

1 Borghetti J, Snider G S, Kuekes P J, et al. Memristive switches enable stateful logic operations via material implication. Nature, 2010, 464: 873-876.

2 Maestro M, Martn-Martnez J, Crespo-Yepes A, et al. Experimental verification of memristor-based material implication NAND operation. IEEE Transactions on Emerging Topics in Computing, 2017, 7(4): 545-552.