SCIENCE CHINA

Information Sciences



November 2021, Vol. 64 219402:1–219402:2 $\label{eq:condition} $\operatorname{https://doi.org/10.1007/s11432-020-3127-x}$$

Investigation of weight updating modes on oxide-based resistive switching memory synapse towards neuromorphic computing applications

Qingting DING^{1,2}, Tiancheng GONG^{1,2}, Jie YU^{1,2}, Xiaoxin XU^{1,2}, Xiaoyan LI¹, Hangbing LV^{1,2*}, Jianguo YANG^{1,2}, Qing LUO^{1,2}, Peng YUAN^{1,2}, Feng ZHANG^{1,2} & Ming LIU^{1,2}

¹Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; ²University of Chinese Academy of Sciences, Beijing 100049, China

Received 24 September 2020/Revised 5 November 2020/Accepted 25 November 2020/Published online 7 September 2021

 $\label{eq:citation} \begin{array}{ll} \text{Citation} & \text{Ding Q T, Gong T C, Yu J, et al. Investigation of weight updating modes on oxide-based resistive switching memory synapse towards neuromorphic computing applications. Sci China Inf Sci, 2021, 64(11): 219402, \\ \text{https://doi.org/}10.1007/\text{s}11432-020-3127-\text{x} \end{array}$

Dear editor,

• LETTER •

Memristors, resistive random access memory (RRAM) devices when used in memory applications, have attracted significant interest recently as a promising candidate for neuromorphic computing systems due to their excellent size scalability, fast switching speed and low energy consumption [1]. In order to obtain high learning accuracy in neural networks based on back propagation learning rule, the updating behavior of synaptic linear symmetric weights is important [2]. During weight update, the resistance of the memristor device can be adjusted incrementally by controlling the distribution of oxygen vacancies, which modulate the overall conductance of the device.

In 1T1R device, the potentiation can be achieved by continuously ramping up the pulse amplitude of gate electrode which called gate voltage ramping (GVR) mode, but the generation of non-identical pulses causes an additional burden to design the peripheral circuitries as well as the latency and power consumption. Constant drain voltage (CDV) mode, which applies a particular sequence of either a single or a pair of pulses on the drain electrode, is proposed to solve this problem, but still suffer from a saturation problem [3]. However, the deeper comparison in reliability of these two different modes are still unclear, especially in retention degradation issue, which will degrade the performance of neural network. Therefore, it is in highly demand to investigate the retention behaviors, aiming at evaluating and optimizing the reliability of RRAM-based neural network.

In this study, the systematic comparison between the low resistance state (LRS) retention characteristics during potentiation process of 1T1R RRAM device, which are programmed by GVR mode and CDV mode respectively, is investigated by time lag plot (TLP) technique. Our results

The 1T1R RRAM cell studied here was fabricated on the 28-nm standard logic platform [4]. Detailed information on the integration process could be found in Appendix A.

The current-voltage (I-V) curves up to 100 cycles in DC switching mode are shown in Figure 1(a), an abrupt transition from the high resistance state (HRS) to the LRS is observed during SET process, while a gradual transition occurred during RESET process, resulting in a binary state. This results from the difference in the switching mechanism between set and reset processes [5]. The asymmetric weight update behavior of synapse significantly reduces the accuracy in pattern recognition and degrades the performance of neural network. Figure 1(b) shows cycle-to-cycle resistance distribution by applying 2.5 V/100 ns SET pulse and -2.5 V/200 ns RESET pulse. The resistances of LRS and HRS are approximately 10 k Ω and 100 k Ω . 10X memory window can be clearly observed and excellent uniformity of HRS and LRS are achieved in the devices.

Two types of pulse schemes shown in Figures 1(c) and (d) are utilized to update the conductance for potentiation. The gate voltage is ramped up to 1.8-2.7~V/100~ns while a fixed SET condition is applied on the drain electrode, which is called GVR mode, as shown in Figure 1(c). Multi-level cells (MLCs) in potentiation can be obtained by gradually increasing the amplitude of gate pulse, thus increasing the compliance current, leading to more oxygen vacancies migrating to the CF. As expected, MLC is achieved by GVR mode. In addition, a linearly changed MLC under a fixed

reveal that, for a given LRS, the retention characteristics under GVR mode is much better than CDV mode. This improvement can be interpreted as the strong percolation network formed under GVR mode. This result is beneficial for choosing the suitable weight update mode of 1T1R RRAM devices towards neuromorphic computing applications.

^{*} Corresponding author (email: lvhangbing@ime.ac.cn)

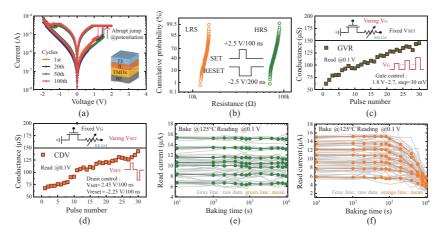


Figure 1 (Color online) (a) I-V curves of the 1T1R RRAM devices for 100 cycles. Inset: schematic of RRAM stack. (b) Cycleto-cycle resistance distribution measured in 100 cycles. (c) Employed nonidentical programming pulse schemes for potentiation. Releasing current limiting gradually results in many oxygen vacancies move to the CF. (d) Optimized programming schemes with identical SET pulse and RESET pulse pair. The increased conductance measured at 0.1 V. High temperature retention measurement (125°C) of incremental LRSs programmed by (e) GVR mode, (f) CDV mode.

Gate voltage and identical pulses on drain electrode can also be obtained by a SET pulse (+2.45~V/100~ns) accompanying a RESET pulse (-2.25~V/100~ns) during potentiation, as shown in Figure 1(d), which is called CDV mode. Optimized SET and RESET pulse can adjust IRS linearly as a function of the pulse number in CDV mode [6].

For a fair comparison, we choose seven states with roughly the same IRSs of each mode respectively to investigate the retention behaviors of potentiation process by GVR mode and CDV mode in 1T1R. Figures 1(e) and (f) show the statistical retention characteristics at 125°C for 10⁴ s of 10 cells. Stable retention is obtained by GVR mode in Figure 1(e), while the retention in CDV mode shown in Figure 1(f) are gradually getting worse after 10³ s baking, indicating that the GVR mode can significantly improve the LRS retention. For the read current obtained in the CDV mode, no significant change in the mean read current was observed during the first 10^3 s baking process, and the mean read current decreased during the subsequent baking process. It worth noting that the mean read current of high current states sharply decrease with time, while the mean read current of low current states show a slightly decreasing trend.

To further understand the impact of different schemes, we introduce RTN (random telegraph noise) measurement and TLP technique [7], the corresponding analysis are summarized in Appendix B.

According to the percolation theory, the characteristic of the percolation path is correlated with the oxygen vacancies concentration [8]. The TLP results reveal that traps interaction surrounding the percolation path is more active for GVR mode than CDV mode. Therefore, under CDV mode, Vo exhibit scattered with low oxygen concentration N(Vo). In such cases, the percolation network is weak, the read current sharply decreases once the Vo diffused and a critical percolation path is cut off, indicating the retention degradation occurs. While in GVR mode, oxygen vacancies (Vo) are gathering at filament region with high N(Vo), a stronger percolation network is achieved. Even though one percolation path cut off, the state could be hold due to the remained strong network. Thus, maintaining sufficient retention can be obtained by GVR mode due to stronger percolation network. This result provides a better solution

for weight update towards neuromorphic computing applications.

Acknowledgements This work was supported by the National Science and Technology Major Project of China (Grant No. 2017ZX02301007-001), National Natural Science Foundation of China (Grant Nos. 61922083, 61804167, 61834009, 61904200, 62025406, 61821091), and Strategic Priority Research Program of Chinese Academy of Sciences (Grant No. XDB44000000).

Supporting information Appendixes A and B. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors

References

- Park S, Kim H, Choo M, et al. RRAM-based synapse for neuromorphic system with pattern recognition function.
 In: Proceedings of International Electron Devices Meeting, 2012
- 2 Chang C C, Chen P C, Chou T, et al. Mitigating asymmetric nonlinear weight update effects in hardware neural network based on analog resistive synapse. IEEE J Emerg Sel Top Circ Syst, 2017, 8: 116–124
- 3 Woo J, Yu S M. Resistive-memory-based analog synapse: the pursuit for linear and symmetric weight update. IEEE Nanotechnol Mag, 2018, 12: 36–44
- 4 Lv H B, Xu X X, Yuan P, et al. BEOL based RRAM with one extra-mask for low cost, highly reliable embedded application in 28 nm node and beyond. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2017.
- 5 Woo J, Moon K, Song J, et al. Improved synaptic behavior under identical pulses using ${\rm AlO}_x/{\rm HfO}_2$ bilayer RRAM array for neuromorphic systems. IEEE Electron Dev Lett, 2016, 37: 994–997
- 6 Woo J, Moon K, Song J, et al. Optimized programming scheme enabling linear potentiation in filamentary $\rm HfO_2$ RRAM synapse for neuromorphic systems. IEEE Trans Electron Dev, 2016, 63: 5064–5067
- 7 Gonzalez M B, Martin-Martinez J, Maestro M, et al. Investigation of filamentary current fluctuations features in the high-resistance state of Ni/HfO₂-based RRAM. IEEE Trans Electron Dev, 2016, 63: 3116–3122
- 8 Ninomiya T, Wei Z, Muraoka S, et al. Conductive filament scaling of ${\rm TaO}_x$ bipolar ReRAM for improving data retention under low operation current. IEEE Trans Electron Dev, 2013, 60: 1384–1389