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• **Supplementary File** •

Investigation of Weight Updating Modes on Oxide-based Resistive Switching Memory Synapse towards Neuromorphic Computing Application

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Appendix A Device Fabrication

The 1T1R RRAM cell studied here was fabricated on the 28-nm standard logic platform. Detailed information on integration process could be found in our previous work [1-2]. The RRAM unit was built between Contact W plug (CT) and Metal 1 (M1) by adding only one non-critical extra mask. A 8-nm TaOx switching layer was formed in the M1 trench, in connection with the CT (bottom electrode, BE). The M1 serves as the top electrode, and in between TaOx and M1 there is an interfacial layer. The cell size is about 40-nm×40-nm.

Appendix B RTN Result And TLP Analysis

To further understand the impact of different scheme, we introduce RTN (Random Telegraph Noise) measurement [3]. After each programming, a RTN measurement was carried out in the 1R cell between TE and BE. RTN was measured under TE bias = 0.1V and the Sampling Rate (SR) $=10^5$ Hz of each testing. The BE was kept grounded. Fig. S1(a) and S1(b) are the multi-level RTN signals of LRS under these two modes, respectively.

In low resistance states, the current fluctuations of RTN is attributed to trapping/de-trapping of carriers in/from a charged trap located in the vicinity of the CF which can block a portion of CF and modulate the effective cross-section of the CF [4]. In neural network applications, these fluctuations will limit the device reliability. In order to investigate the mechanisms responsible for current fluctuations and to check the active traps interaction in the filamentary conductive path, we employed TLP (Time Lag Plot) technique which consists in plotting the current value at a certain moment (current at i+1) versus the previous value (current at i). Note that the current fluctuations can only be observed when charge trapping occurs in the time window of the measurement setting.

The corresponding TLPs are shown in Fig. S1(c) and S1(d). The points in the diagonal of the Time Lag Plot indicate the RTN current levels which is attributed to the different charge states, while points outside the diagonal represent the interaction between different states. The TLP color bar indicates the probability to find a current value in the current at i and current at i+1 plane. These additive current fluctuations shown in Fig. S1(b) could be understood as no obvious interactions between traps which can modulate the percolation path individually. Non-correlated transitions can be observed under CDV mode as shown in Fig. S1(d), which are the result of the contribution of independent traps altering the percolation path. As a contrast, the traps interaction is more active under GVR mode as shown in Fig. S1(c), which indicates that the localized traps are spaced closely and the trap fluctuations may involve changes in the occupation probability of other traps. Therefore, multilevel fluctuations with a complex dynamical process are detected. Thus, the localization of the filament paths under GVR mode can be confirmed.

References

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