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Design of a high-performance 12T SRAM cell for single event upset tolerance

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Dear editor,

As an important part of a cache, static random-access memory (SRAM) has been extensively utilized to satisfy the application requirements in modern embedded processors. It plays an important role in data interaction between the central processing unit and internal memory. Moreover, these data interactions are safety critical requiring highly reliable SRAM. However, owing to complementary metal-oxide-semiconductor (CMOS) manufacturing processes entering the nanoscale era, SRAM is increasingly vulnerable to a single event upset (SEU).

In this study, a high-performance 12T SRAM cell (HP12T) with lower power consumption for SEU tolerance is proposed and verified by conducting a simulation using a 65 nm CMOS commercial technology. By applying a reasonable circuit-level and layout-level design, HP12T SRAM cell can tolerate an ion striking on any of its sensitive nodes with LET = 99.8 MeV-cm^2/mg at normal strike.

Figure 1(a) demonstrates the basic schematic structure of the proposed HP12T SRAM cell. It employs 12 transistors, where p-type metal-oxide-semiconductor (PMOS) transistors P1–P4 and n-type metal-oxide-semiconductor (NMOS) transistors N1–N2 are pull-up transistors, NMOS transistors N3–N4 and N7–N8 are pull-down transistors, and NMOS transistors N5–N6 are access transistors. Additionally, these transistors form four stored nodes, that is, nodes Q, QN, S1, and S0. The word line WL is connected with the gates of the two access transistors at the same time; meanwhile, the bit lines BL and BLN are connected with the drains (or sources) of the access transistors, respectively.

First, the basic functions of access and hold operations of HP12T SRAM cells are verified by conducting a simulation. Therefore, a memory with a 1-bit storage capacity is designed. Further, by applying models derived from a 65 nm CMOS commercial technology with 1.2 V power supply, typical process corner, and at room temperature, a set of access and hold operations are simulated. As shown in Figure 1(b), our simulation results confirm that HP12T SRAM cell can correctly achieve the read, write, and hold operations.

SEU physical mechanism indicates that radiation-induced current can only flow from n-type to p-type diffusion through a p-n junction because of its reverse bias. This means that if a susceptible node comprised only PMOS transistors, a radiation particle strike cannot change the node voltage from 1 to 0; similarly, if a susceptible node comprised only NMOS transistors, the node voltage cannot flip from 0 to 1. Therefore, under the assumption of Q = 1, QN = 0, S0 = 1, and S1 = 0 combined with SEU physical mechanism, node QN is not a susceptible node when an energetic particle strikes on. Thus, the HP12T SRAM cell has three susceptible nodes (Q, S0, and S1). Moreover, the SEU recovery behavior is analyzed as follows.

(1) If an SEU occurs on node Q, the state of node Q is changed from 1 to 0. This temporarily turns off transistors N4 and N7 and turns on transistor P4. However, these changes cannot affect nodes QN, S0, and S1. Consequently, node Q will finally be returned to its original state 1.

(2) If an SEU occurs on node S1, the state of node S1 is changed from 0 to 1. This temporarily turns off transistor P1 and turns on transistor N2. These changes cannot affect nodes Q and S0. However, the competition of charging or discharging node QN between transistors N2 and N7 occurs, that is, transistor N2 will charge node QN while transistor N7 will simultaneously discharge node QN. Based on SRAM access-operating principle, the pull-down transistor employs the largest size transistor, the access transistor is the next, and the pull-up transistor employs the smallest size transistor. It can be easily deduced that the pull-down ability of transistor N7 is much better than the pull-up ability of transistor N2. Besides, charging node QN through transistor N2 is a weakly driven process, whereas discharging node QN through transistor N7 is a much stronger driven process. These two mechanisms ensure that node QN can hold its original state 0. Since nodes Q, QN, and S0 are all at their original states, node S1 will finally be returned to its original state 0.

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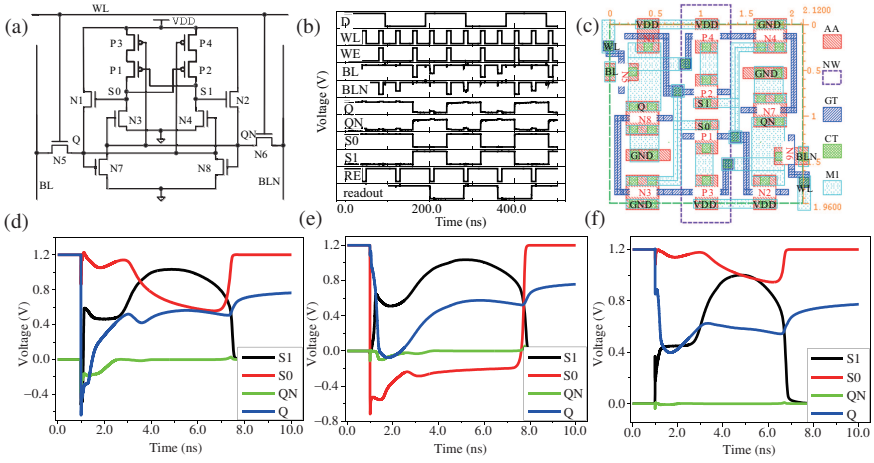

(g)

SRAM type	Critical charge (fC)		Performance (normalized to 6T)				Static noise margin (mV)		
	SEU	SEDU	Aera	Static power	Write delay	Read delay	RSNM	WSNM	HSNM
6T	No data		1	1	1	1	272.3	399.5	424.7
NS10T			2.1	2.65	1.37	1.27	126.7	388.3	685.8
PS10T			2.41	1.37	1.45	1.04	231	463.5	565.6
Quatro10T	68.67	17.06	2.2	3.44	1.68	1.03	292	257.7	687
DICE	–	16.64	2.5	1.95	0.87	0.81	525	429.6	875
13T	No data		3.33	2.33	2.82	0.82	307.5	623.5	502.5
RHMP			3.45	2.71	1.44	2.43	550	448	686.5
RHMN	–	8.23	2.74	1.85	1.52	1.03	16.5	489.6	566.5
HP12T	–	>25.49	2.75	0.8	1.26	1.05	497.7	585	615.2

Figure 1 (Color online) (a) Schematic diagram of the proposed HP12T SRAM cell; (b) normal operation diagram of HP12T SRAM cell; (c) the layout of HP12T SRAM cell; (d) ion striking on node Q; (e) ion striking on node S0; (f) ion striking on node S1; (g) comparisons of different SRAMs' performance (please refer to [1] for understanding the structure of each SRAM cell listed here).

(3) If an SEU occurs on node S0, the state of node S0 is changed from 1 to 0. This temporarily turns on transistor P2 and turns off transistor N1. However, these changes cannot affect nodes Q, QN, and S1. Consequently, node S0 will finally be returned to its original state 1.

Figure 1(c) depicts the layout design of the HP12T SRAM cell. Here, to mitigate the upset from 0 to 1 (occurring on node S1), the special circuit level design of stacking transistors P1 and P3 (also P2 and P4) can enable HP12T SRAM cell use the layout technique via the source isolation [2]; PMOS transistor P1 (P2) is directly isolated from transistor P3 (P4) by a shallow trench isolation (STI) whose width is 240 nm. Besides, the well contacts are inserted between transistors N3 (N4) and N8 (N7) to isolate nodes Q (QN) and S0 (S1), essentially weakening the charge-sharing effect between them. These two special robust designs at the layout level will make the HP12T SRAM cell much stronger.

The SEU hardened ability of HP12T SRAM cell is investigated by conducting technology computer aided design (TCAD) mixed-mode simulations with heavy-ion striking on nodes Q, S0, and S1 at LET = 99.8 MeV-cm^2/mg. Here to consider the charge-sharing effect, all the off transistors except for access transistors N5 and N6 are designed in the TCAD model, and the positions are the same since they are in layout. Figures 1(d)–(f) illustrate the TCAD mix-mode simulation results. We can observe that HP12T SRAM cell can tolerate ion strikes with LET = 99.8 MeV-cm^2/mg even though the charge-sharing effect is considered.

Figure 1(g) shows the comparison of critical charges of DICE (dual interlocked storage cell), Quatro10T, RHMN, and HP12T SRAM cells. Since the charge-sharing effect is related to the distances between the arbitrary two nodes in the layout, for a fair comparison, the SEU and single event double node upset (SEDU) critical charge of DICE, Quatro10T, and RHMN are directly obtained from reference [3]. It can be observed that only Quatro10T cell cannot fully tolerate SEU, whereas others can fully tolerate SEU. Further, when considering the charge-sharing effect, the HP12T SRAM cell possesses a much better ability to SEDU tolerance. Figure 1(g) also depicts the comparisons of performance and SNMs (static noise margins) of different SRAM cells. Generally, higher radiation hardness could be achieved by applying the radiation hardened by design (RHBD) method. In exchange, more transistors are required at circuit level design, which inevitably leads to an increase in area. Therefore, it is a trade-off between radiation hardness and performance in SRAM cell design. Although HP12T SRAM cell does not have an absolute advantage on area overhead, access time, and SNMs, analyzing Figure 1(g) demonstrates a better composite indicator when considering the main purpose of this design (that is, SEU tolerance and low power).

Conclusion. This study proposed a lower power RHBD HP12T SRAM cell. We obtained the following results about HP12T SRAM cell: (1) it can successfully complete normal access and hold operations; (2) it can tolerate heavy-ion striking with LET = 99.8 MeV-cm^2/mg even though the charge-sharing effect is considered; (3) it has lower power consumption and comparable access time and SNMs when compared with classical and state-of-the-art SRAM cells.

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