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Nano-scaled transistor reliability characterization at nano-second regime

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Dear editor,

In recent years, novel MOSFET structures such as fully-depleted silicon-on-insulator (FDSOI) MOSFET and FinFET are adopted by the industry for their excellent electrostatic behavior and higher on-state current per footprint. Nevertheless, these novel structured transistors suffer from severe self-heating effects (SHE) owing to the more heat generation but lower thermal conductivity of the ultrathin Si channel [1]. Not only does SHE degrade the device performance and reliability, but also it imposes additional challenges inaccurate device characterization [2]. For example, the severe SHE generated in the time-consuming measurement process will affect the accurate interpretation of reliability lifetime [3]. Among all the degradation issues of the nano-scaled transistors, hot carrier injection (HCI) is considered a widely concerned problem for nMOSFETs. Accurate extraction methodology is required to obtain the precise HCI degradation parameters, namely, $\Delta V_{\rm TH}$ and $\Delta I_{\rm DSAT}$, which are highly dependent on the channel temperature and the trapping-detrapping process of interface defects [4]. To exempt the effect of both factors, reducing measurement time to the nano-second regime is essential [5].

In this study, the effect of measurement speed (from μs to sub-ns scale) on the reliability characteristics of the nano-scaled FDSOI MOSFETs was studied. An ultra-fast pulse *I-V* measurement (UFM) system was utilized to eliminate SHE and trapping effect to the highest extend. HCI degradation characteristics were investigated to study the impact of SHE and trap response on the device reliability. In addition, an optimal measurement methodology is proposed as the benchmark of the characterization for nano-scaled transistor performance and reliability. In this experiment, a self-developed nanosecond-scale UFM system [6] was used for the electrical measurement, as shown in Figure 1(a). The detailed setup of the UFM system could be found in [6]. For the UFM system, the pulse width for measurement could reach the sub-1 ns regime and the accuracy of the oscilloscope could reach 10 ps.

FDSOI nFETs with high-κ/metal gate (HKMG) technology were fabricated and used in this work. Ultrathin body and buried oxide (UTBB) wafers were used for the fabrication of FDSOI devices. The Si layer thickness was within 10 nm and the BOX layer thickness $T_{\rm BOX}$ was ∼12 nm. The fabrication processes for the FDSOI devices followed the standard Si processing technologies [7]. HKMG technology was used for the fabrication of gate stack. The high-κ layer mainly consists of elements Si, O, N and Hf. The physical thickness of the high-κ layer is ∼4 nm and the estimated EOT is ∼1 nm. The gate width W_G and length L_G used here were 12 μm and 30 nm, respectively.

For the stress phase in HCI characterization, the signal generator was responsible to provide the gate stress with various types of patterns, namely, DC, high-frequency AC and PRBS signals. In the measurement phase, I_D-V_G plots were characterized under various measurement speeds. For each data point in the I_D-V_G curve, data averaging was used to avoid the effect of system noise on the data accuracy. I_D response to the periodic gate pulse was averaged over several periods at each V_G and V_D value to obtain a more noise-free current value.

"Measure-Stress-Measure" procedure was carried out on the above-mentioned SOI nMOSFETs with L_G = 30 nm. $V_{\rm Gstress} = V_{\rm Dstress}$ = 1.1 V was chosen as the stress condition. In the measurement phase, I_D-V_G pulse measurement was carried out under five different measurement speeds from 800 ps to 1 ms for the extraction of $\Delta V_{\rm TH}$ and $\Delta I_{\rm DSAT}$. Figure 1(b) shows the change of HCI-induced $I_{\rm DSAT}$ drifting as a function of the stress time $t_{\rm stress}$. Here, $I_{\rm DSAT}$ was extracted by constant voltage method at a voltage level of 0.8 V. In general, $I_{\rm DSAT}$ decreases as $t_{\rm stress}$ increases. The HCI-induced degradation measured at shorter characterization pulse width is higher than that at a long measurement

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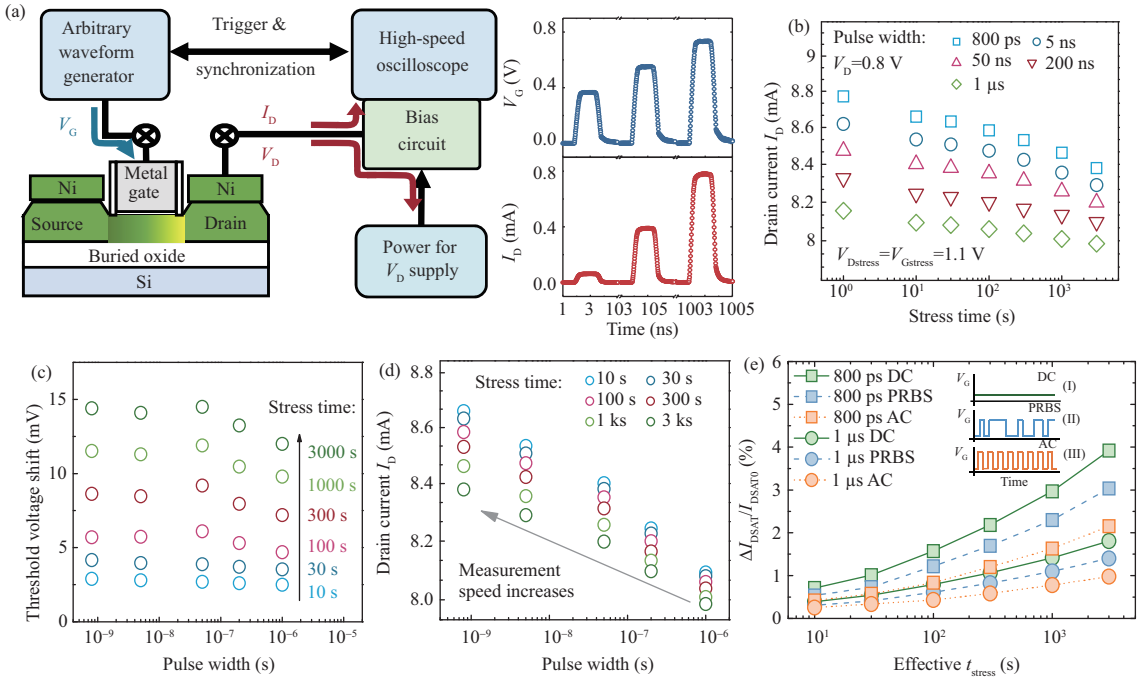

Figure 1 (Color online) (a) Schematic of the ultra-fast measurement system used in this study. Pulses with different pulse widths were used to capture the *I-V* characteristics. Ultra-fast gate pulses V_G generated by AWG and the corresponding drain response I_D used in the experiment. Both are with a width longer than 800 ps. (b) I_{DSAT} changing as a function of HCI stress time. SOI nMOSFETs (L_G = 30 nm, W_G = 12 µm) were stressed for 3000 s. (c) Comparison of ΔV_{TH} changing as a function of pulse width with different measurement times using ultra-fast pulse *I-V* measurement. (d) Comparison of I_{DSAT} changing as a function of pulse width with different measurement times using ultra-fast pulse *I-V* measurement. (e) $\Delta I_{DSAT}/I_{DSAT0}$ degradation with three different stress patterns as a function of the effective t_{stress}, characterized with pulse width 800 ps.

pulse width. Therefore, the long measurement time will underestimate the HCI-induced degradation, leading to an overestimation of the predicted HCI lifetime.

Figures 1(c) and (d) plot the HCI-induced ΔV_{TH} and I_{DSAT} change with respect to the measurement speed (shown as pulse width). Here, V_{TH} was extracted by constant current method at a current level of $(W_G/L_G)\times 600$ nA. Similar to Figure 1(b), for FDSOI nMOSFETs, the measurement speed exhibits a strong impact on the characterization of reliability behaviors. The HCI induced ΔV_{TH} increases as measurement speed increases, as shown in Figure 1(c). In fact, measurement speed induced V_{TH} variation is involved in the I_D-V_G measurements both before and after stress. One possible explanation for the trend shown in Figure 1(c) could be as follows: $\Delta V_{TH} = V_{TH,After} - V_{TH,Before}$, where $V_{TH,After}$ and $V_{TH,Before}$ both decrease as measurement speed increases (or pulse width decreases). If $V_{TH,After}$, or in other words, the HCI-induced traps are less sensitive to measurement speed than V_{TH}, before where only intrinsic traps exist, ΔV_{TH} will increase as the measurement speed increases. In addition, since longer pulse width results in more SHE, the decreased ΔV_{TH} at a longer measurement speed may also be due to the faster trapping-detrapping process at an elevated channel temperature. However, further investigation needs to be done to support the above-mentioned hypotheses. The observations in Figures 1(c) and (d) strongly indicate that nanosecond level measurement speed is necessary for precise extraction of reliability parameters, in order to predict a precise reliability lifetime in FDSOI MOSFETs.

The impact of gate stress waveforms, namely, static DC (Figure 1(e)(I)), periodic AC (Figure 1(e)(II)) and pseudo-random binary sequence (PRBS) (Figure 1(e)(III)) signals, on the HCI induced degradation, was tested for the FDSOI nMOSFETs. The periodic AC waveform with a frequency of 5 GHz was used with an amplitude of 1.1 V. The PRBS stress pattern was adopted to mimic the irregular switching process in the "real" IC operations [8], which has a sequential length of $(2^{15}-1)$ bits and a bit frequency of 5 GHz.

Figure 1(e) compares the degradation results from measurements with measurement speeds of 800 ps and 1 µs. The worst case is the DC bias scenario, which is more serious than the other two cases even with the same effective t_{stress}. Furthermore, the degradation in the PRBS case is more significant than the AC case, possibly owing to some continuous 1 bit in the PBRS stress patterns causing stronger SHE.

In this study, the effect of measurement speed on the reliability degradation in nano-scaled FDSOI transistors was studied. Owing to the serious SHE and defect trapping in the measurement and stress phases, both V_{TH} and I_{DSAT} shift were underestimated by the DC or low speed pulsed *I-V* test, leading to an overestimated prediction of HCI lifetime. In addition, the HCI reliability of FDSOI MOSFETs is much better when under AC and PRBS HCI stress, as compared with that under DC bias. The developed methodology demonstrated here could also be applied to study the reliability of nano-scaled transistors with new structures or novel channel materials where SHE and interfacial traps have to be considered.

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