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High mobility germanium-on-insulator p-channel FinFETs

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Dear editor,

Over the past decade, germanium has attracted great interest as a promising channel material for p-channel metal oxide semiconductor field-effect-transistor (MOSFET), owing to its higher hole mobility over Si [1]. Tremendous efforts were devoted to solving the technical issues for its practical applications, including source/drain (S/D) ohmic contact formation, strain engineering, channel surface passivation, and gate dielectric engineering [2]. In particular, it is reported that the the effective hole mobility ($\mu_{\rm eff}$) of Ge pMOSFET can be effectively enhanced by the reduced density of interface trap via gate dielectric engineering [3].

ZrO_2, one of the most promising dielectric materials [4,5], demonstrates both excellent dielectric properties and ferroelectricity, which play a critical role for future CMOS technology in 'More than Moore' era [6]. Studies have shown that a GeO_2 interfacial layer can decompose and intermix with the ZrO_2 layer during thermal annealing, decreasing CET [7]. However, there is still a lack of experimental investigation on Ge p-channel FinFETs with ZrO_2 dielectric.

In this study, Ge p-channel FinFETs with ZrO_2 dielectric are fabricated on (100)-oriented germanium-on-insulator (GeOI), which demonstrates the improved $\mu_{\rm eff}$ compared to Si universal mobility. The impacts of fin direction on the electrical performance of the devices are also discussed.

Device fabrication. GeOI wafer with 100 nm top Ge(100) film and ∼150 nm buried oxide is used for the FinFET fabrication. A phosphorous ion (P^+) implantation with a dose of 1×10^{13} cm^{-2} and an energy of 45 keV is carried out, followed by the thermal annealing at 700°C to form the n-well. And then, S/D regions were defined and implanted using BF_2^+ with a dose of 1×10^{15} cm^{-2} and an energy of 30 keV. After that, dry etching is used to reduce the top Ge to about 50 nm. Fins are formed by the patterning using e-beam lithography and dry etching. After a pre-gate cleaning, the wafers are loaded into an atomic layer deposition chamber for the formation of the 4.5 nm ZrO_2 gate dielectric layer at 300°C. $Zr[N(CH_3)_2]_4$ and H_2O are used as the precursors of Zr and O, respectively. During deposition, the $Zr[N(CH_3)_2]_4$ source is heated to 85°C. Subsequently, a TaN gate layer is deposited. After this layer is patterned to form the gate electrodes, Nickel S/D metal electrodes are then formed by a lift-off process into S/D regions. Finally, thermal annealing at 450°C for 30 s is carried out for the S/D dopant activation and improvement of the gate stack.

Figure 1(b) shows the top-view scanning electron microscope (SEM) image of the fabricated Ge pFinFET on GeOI. Figure 1(c) shows the transmission electron microscope (TEM) image of pFinFET with several parallel fins. High-resolution TEM (HRTEM) in Figure 1(d) demonstrates that fin with ($W_{\rm fin}$) and fin height ($H_{\rm fin}$) are 30 nm and 33 nm, respectively, which is surrounded by the interfacial layer of GeO_x and the dielectric of ZrO_2.

Results and discussion. Figure 1(e) shows the measured drain current ($I_{\rm DS}$) vs. gate voltage ($V_{\rm GS}$) curves at different drain voltage ($V_{\rm DS}$) for a pair of GeOI pFinFETs with fin directions of [110] and [100]. Similar subthreshold swing (SS) of 160 mV/decade and ON to OFF current ratio ($I_{\rm ON}/I_{\rm OFF}$) of 5 orders is observed for the two channel directions, indicating the same fin dimension of the devices. SS of the GeOI FinFETs can be reduced by optimizing the surface passivation and decreasing the $W_{\rm fin}$ of the devices. The $I_{\rm DS}$-$V_{\rm DS}$ curves at different gate overdrive $|V_{\rm GS} - V_{\rm TH}|$ in Figure 1(f) show that drive current in device with [110] fin direction is higher than that of the transistor with [100] channel direction. Here, $V_{\rm TH}$ is defined as $V_{\rm GS}$ corresponding to $I_{\rm DS} = 10^{-7}$ A/μm. The boosted $I_{\rm DS}$ for [110] fin device is attributed to an improved $\mu_{\rm eff}$.

Figure 1(g) shows the statistical plots for total on-state resistance ($R_{\rm tot}$) of GeOI pFinFETs with fin directions of [110] and [100], measured at a gate overdrive of 1.5 V and $V_{\rm DS}$ of −0.05 V. S/D resistance ($R_{\rm SD}$) and channel resistivity $\Delta R_{\rm tot}/\Delta L_{\rm G}$ are extracted from the y-intercept and slope of this plot, respectively. The same RSD of ∼3 kΩμm is obtained for the devices with different channel directions. $\Delta R_{\rm tot}/\Delta L_{\rm G}$ related to the inversion charge density ($Q_{\rm inv}$) and $\mu_{\rm eff}$ are extracted to be 4.6 and 5.5 kΩ for [110] and [100] FinFETs, respectively. $Q_{\rm inv}$ is calculated from the inversion capacitance ($C_{\rm inv}$) vs. $V_{\rm GS}$ curves in Figure 1(h). GeOI FinFETs have a capacitance equivalent thickness (CET) value

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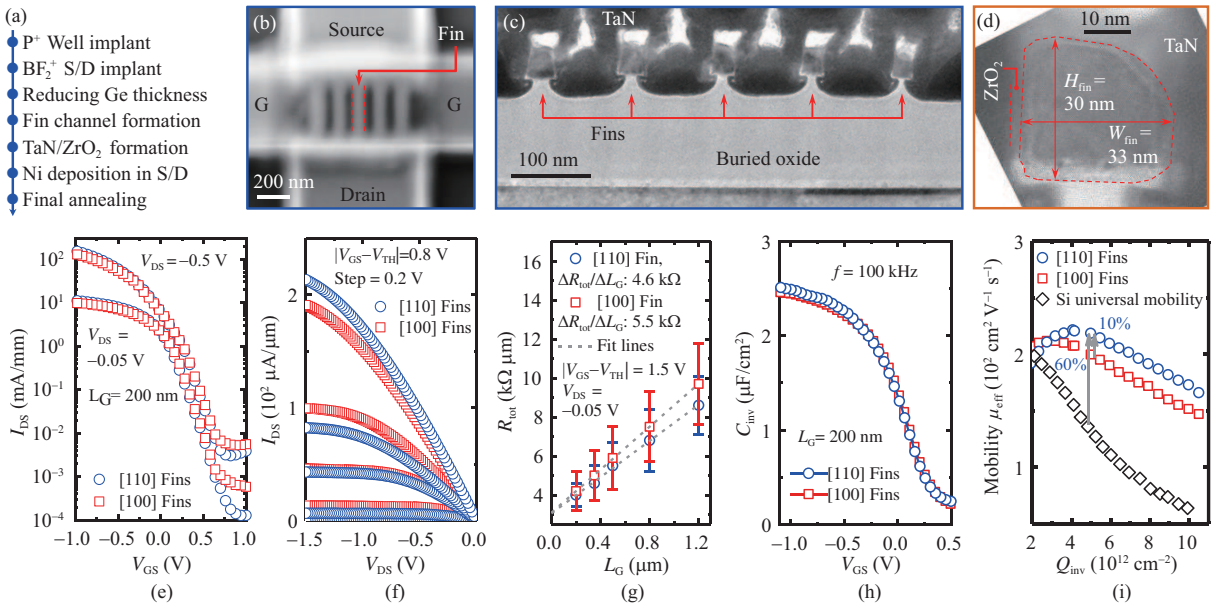

Figure 1 (Color online) (a) Key process steps for fabricating GeOI FinFETs; (b) SEM and (c) TEM images of GeOI FinFETs with parallel fins; (d) HRTEM showing a Ge fin with $W_{\rm fin}$ of ∼33 nm and Hfin of ∼30 nm; (e) measured $I_{\rm DS}$-$V_{\rm GS}$ curves of a pair of GeOI FinFETs with fin directions of [110] and [100]; (f) $I_{\rm DS}$-$V_{\rm DS}$ curves showing that device with fin direction of [110] has a higher $I_{\rm DS}$ compared to the transistor along [100]; (g) $R_{\rm tot}$ vs. $L_{\rm G}$ for GeOI FinFETs measured at $|V_{\rm GS}-V_{\rm TH}|=1.5$ V and $V_{\rm DS}=-0.05$ V; (h) $C_{\rm inv}$-$V_{\rm GS}$ characteristics measured at a frequency of 100 kHz for the GeOI FinFETs; (i) $\mu_{\rm eff}$ vs. $Q_{\rm inv}$, extracted using the split C-V method. Higher $\mu_{\rm eff}$ is achieved in GeOI FinFETs compared to Si universal mobility.

of 1.5 nm, owing to the high κ value of 23∼25 of ZrO_2 dielectric [4].

$\mu_{\rm eff}$ as a function of $Q_{\rm inv}$ curves calculated as $1/[WQ_{\rm inv}(\Delta R_{\rm tot}/\Delta L_{\rm G})]$ is shown in Figure 1(i), which demonstrates that GeOI FinFETs have a significantly improved $\mu_{\rm eff}$ compared to Si universal mobility. GeOI FinFETs with channel direction of [110] have a 10% improved $\mu_{\rm eff}$ at a Qinv of 5×10^{12} cm^{-2} in comparison with transistors along [100] direction. It was experimentally demonstrated that (110)-oriented Ge p-channel transistors have a higher hole mobility than that of the devices on (100) surface [8, 9]. Furthermore, it was found that [110] fins have a better sidewall surface roughness compared to the [100] fins during the device fabrication, which might lead to an even higher $\mu_{\rm eff}$ in [110] GeOI transistors.

Conclusion. We fabricated and investigated the electrical characteristics of Ge pFinFET on (100)-oriented GeOI wafer. Transistors with fin channel along [110] direction demonstrate the improved drive current and channel $\Delta R_{\rm tot}/\Delta L_{\rm G}$ compared to the devices along [100] direction. At a $Q_{\rm inv}$ of 5×10^{12} cm^{-2}, GeOI FinFETs along [110] direction have 60% and 10% improved $\mu_{\rm eff}$ in comparison with [100] devices and Si university mobility, respectively.

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