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# Simulations of single event effects on the ferroelectric capacitor-based non-volatile SRAM design

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Dear editor,

Non-volatile static random access memory (nvSRAM) with a 6-transistor 2-ferroelectric capacitor (6T2C) structure has been proposed, which meets requirements such as high operating speed and non-volatile memory of the spacecraft and has a wide application prospect in the aerospace field [1, 2]. The single event effects (SEEs) in integrated circuits result from the impact of energetic particles on sensitive areas, which may cause the instantaneous interruption of circuit operation, change in logic state, or even permanent damage to semiconductor integrated circuits [3, 4]. However, the influence of SEEs on nvSRAM based on the ferroelectric capacitor (FeCap) still remains unknown.

In this study, the nvSRAM cell is implemented using a combination of complementary-metal oxide-semiconductor (CMOS) transistors and $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitors. A FeCap macro-model suitable for Hafzirconium-based ferroelectric material is used to simulate the $Hf_{0.5}Zr_{0.5}O_2$ FeCap. Compared with traditional static random access memory (SRAM), the proposed nvSRAM features three main stages of operation: store, power-off, and recall. An independent double exponential current pulse is used to simulate the single-event transient current. By applying transient current pulses to the specified sensitive node of the 6T2C memory cell, upsets in logic "1" or "0" states are observed under different operating conditions. The techniques to mitigate SEEs on the proposed nvSRAM are then addressed by changing the key parameters of the FeCap model.

*Experiment setup.* An $Hf_{0.5}Zr_{0.5}O_2$ FeCap macro-model was proposed for the 6T2C memory cell. The flow chart for building the model is presented in Figure 1(a). The details can be found in previously published studies [5, 6]. The P-V curve obtained from the macro-model simulation is compared with the measured P-V curve of $Hf_{0.5}Zr_{0.5}O_2$ FeCap at different voltages as shown in Figure 1(b). The results show that the simulation results of the built model fit very well with the actual test results. An independent double exponential current pulse, as shown in Figure 1(c), is used to model the heavy ion induced single-event current injection in the specified circuit nodes [7]. The proposed 6T2C nvSRAM simulation circuit is presented in Figure 1(d), which consists of three parts, including the 6T2C nvSRAM cell, the read-write circuit and the precharge circuit. A 1.8 V typical MOS transistor obtained from Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm CMOS process is used in the simulation. The double exponential transient pulse is applied to the junctions of transistors T1 and T2 in Figure 1(d), the "hold on", "store", "power-off", and "recall" states are injected sequentially by changing the "rise time start" value of the transient pulses.

*Simulation results and discussion.* A full operational cycle for the proposed nvSRAM cell uses the following sequence under the control of power supply voltage ($V_{\rm PWR}$) and plate line voltage ($V_{\rm PL}$): "write", "hold on", "store", "power-off", "recall", and "read". The timing chart of nvSRAM operation is shown in Figure 1(e). The double exponential current pulse of linear energy tranfer (LET) = 30 $\mathrm{MeV\cdot cm^2/mg}$ is applied to the "power-off" stage at $T = 555$ ns and $T = 560$ ns. The simulation results are provided in Figure 1(f). When the double exponential pulse is applied at $T = 555$ ns, $V(\mathrm{N1}) = -356$ mV before the power is restarted, and $V(\mathrm{N1}) > V_{\rm th}$ (voltage threshold), the recall operation can successfully recall the data. However, if the pulse is applied at $T = 560$ ns, $V(\mathrm{N1}) = -388$ mV before the power is restarted and $V(\mathrm{N1}) < V_{\rm th}$, an error occurs in the recalled data. Therefore, whether the data can be recalled successfully depends on the injection time of the double exponential transient pulse in the "power-off" phase.

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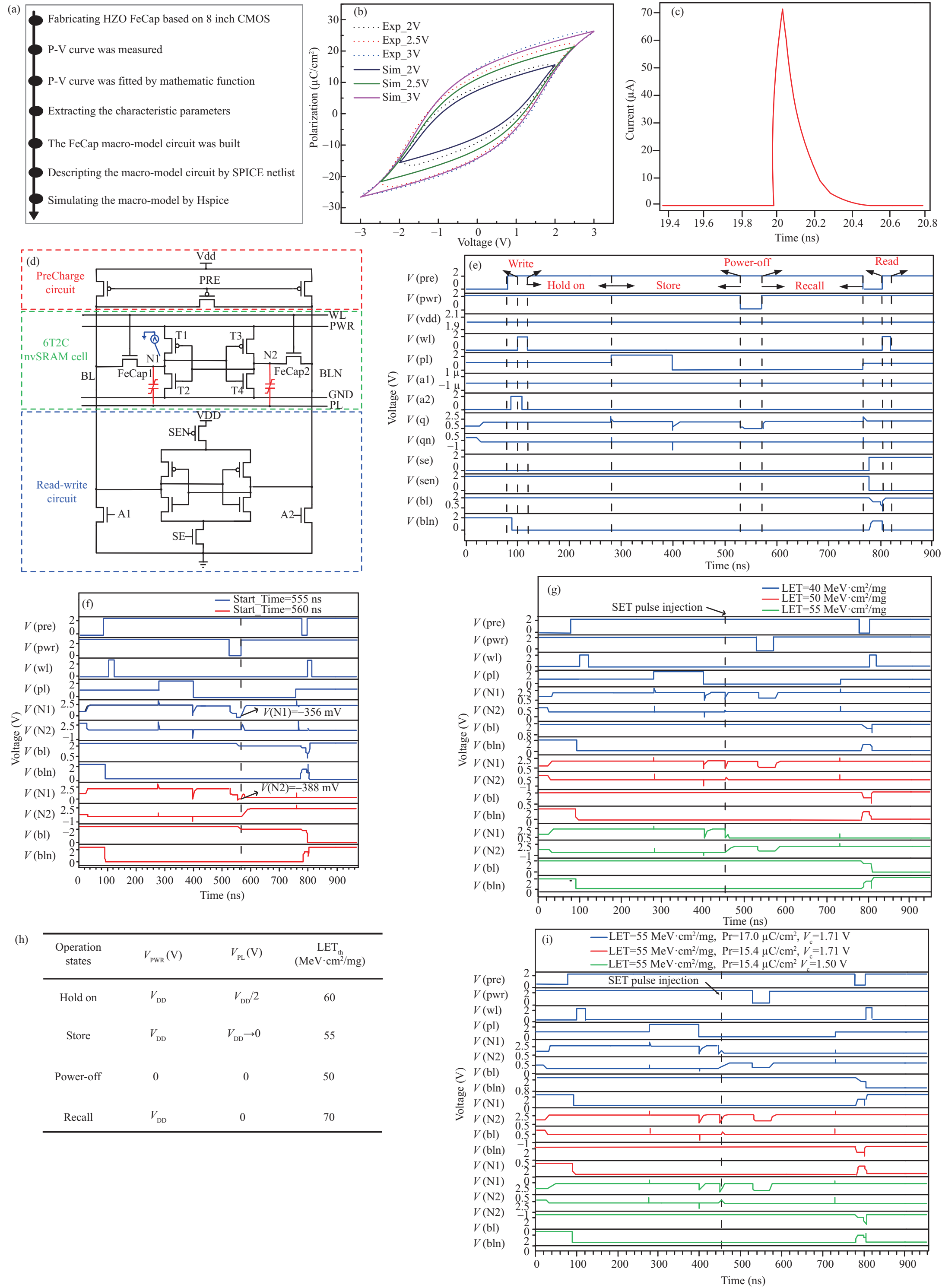


(h)

| Operation states | $V_{PWR}$ (V) | $V_{PL}$ (V) | $LET_{th}$ (MeV·cm²/mg) |
|---|---|---|---|
| Hold on | $V_{DD}$ | $V_{DD}/2$ | 60 |
| Store | $V_{DD}$ | $V_{DD}\rightarrow 0$ | 55 |
| Power-off | 0 | 0 | 50 |
| Recall | $V_{DD}$ | 0 | 70 |

**Figure 1** (Color online) Simulation results of single event effects of nvSRAM in different operating states. (a) Flowchart for building the FeCap model; (b) experimental results and macro-model simulation results for FeCap at different voltages; (c) independent double exponential current pulses; (d) 6T2C nvSRAM simulation with a peripheral circuit; (e) schematic of the timing chart of the nvSRAM operation; (f) double exponential pulses at $T = 555$ ns and 560 ns in the “power-off” state; (g) double exponential current pulses with different LET values in the “store” state; (h) threshold LET values under different operating states; (i) double exponential current pulses applied in the “store” phase under different FeCap model parameters.

Under the influence of double exponential current pulse injection, the flipping of the logic state of the nvSRAM strongly depends on LET. Double exponential current pulses with different LET values in the 30–70 $\mathrm{MeV \cdot cm^2/mg}$ range are applied under different operating conditions, when the LET of the applied pulse is less than the threshold LET ($\mathrm{LET_{th}}$), that is $\mathrm{LET} < \mathrm{LET_{th}}$, the data can be recovered after a short period of disturbance, and the final read data are still correct. However, if $\mathrm{LET} > \mathrm{LET_{th}}$, the data becomes permanently flipped, resulting in soft errors. The simulation results of double exponential pulses with different LET values in the "store" state are shown in Figure 1(g). When the nvSRAM circuit operates in different states, the ferroelectric capacitances are also in different polarization states, leading to different capacities of the circuit to resist the SEEs. Thus, the threshold LET values vary for different operation states. In accordance with the simulation results, the corresponding threshold LET under different operating states is summarized, as shown in Figure 1(h).

Remnant polarization ($P_r$) and coercive voltage ($V_c$) are critical parameters for the ferroelectric performance of ferroelectric thin films. The key parameters of the FeCap model considerably affect the SEEs of nvSRAM. Double exponential current pulses with $\mathrm{LET} = 55\ \mathrm{MeV \cdot cm^2/mg}$ are applied in the "store" phases; critical parameters of the FeCap model are $V_c = 1.71$ V and $P_r = 15.4\ \mathrm{\mu C/cm^2}$; the data cannot be recovered after flipping. By adjusting the critical parameter to $\mathrm{Pr} = 17\ \mathrm{\mu C/cm^2}$ or $V_c = 1.5$ V, the data can be recovered after a short flip, and the final reading data is correct. The simulation results are presented in Figure 1(i). Therefore, the increase in residual polarization intensity or the decrease in the coercive voltage can mitigate the SEEs in nvSRAM.

*Conclusion.* The SEEs on a ferroelectric $\mathrm{Hf_{0.5}Zr_{0.5}O_2}$ capacitor-based nvSRAM have been simulated and analyzed. In the "power-off" phase, whether the data can be recalled successfully depends on the injection time of the double exponential transient pulse. In addition, LET significantly affects the transient radiation responses of nvSRAM, if the LET value of the applied transient pulse is greater than the threshold LET, the data can be permanently flipped, resulting in soft errors. Given this observation, we can mitigate the SEEs on nvSRAM by optimizing the coercive voltage, residual polarization intensity, which are important parameters of the ferroelectric capacitor. These observations are useful for developing novel nvSRAM technologies aiming at space and defense applications..

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