SCIENCE CHINA
Information Sciences

April 2021, Vol. 64 140408:1–140408:3
https://doi.org/10.1007/s11432-020-3155-7

• LETTER •
Special Focus on Two-Dimensional Materials and Device Applications

A compact model for transition metal dichalcogenide field effect transistors with effects of interface traps

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Received 8 November 2020/Revised 4 January 2021/Accepted 6 January 2021/Published online 8 March 2021

Citation Xu Y F, Li W S, Fan D X, et al. A compact model for transition metal dichalcogenide field effect transistors with effects of interface traps. Sci China Inf Sci, 2021, 64(4): 140408, https://doi.org/10.1007/s11432-020-3155-7

Dear editor,

Two-dimensional transition metal dichalcogenide (TMD) materials, such as molybdenum disulphide (MoS_2), are considered as promising channel candidates in field effect transistors (FETs) for future generations of complex systems owing to their ultrathin body and dangling-bond free surface [1]. In this context, a compact model for TMD FETs is indispensable for circuit explorations and designs. In particular, a converging model that can reproduce the sub-threshold and strong-inversion characteristics is important to efficient circuit design for complex digital systems [2].

Interface traps are inevitable in TMD FETs [3,4]. However, in previously published models, they were neglected in [5,6], or a large amount of numerical calculations [7,8] were unavoidable which can introduce the convergence problem. In this study, we propose a converging compact model by simplifying the energy distribution of interface traps. Without a large amount of numerical calculations, our model provides a good fit to experimental results in both sub-threshold and strong-inversion regions and is suitable for efficient circuit explorations for future complex digital systems.

Figure 1(a) shows the schematic of a top-gate FET with a monolayer MoS_2 as its active channel. The channel length and width are L and W, respectively. The source and drain electrodes contact the MoS_2 and are assumed to be ohmic. The source is grounded and considered as the reference potential in the FET. With the voltages applied at the gate electrode (V_{gs}) and the drain electrode (V_{ds}), the current (I_{ds}) flows in the x direction along the channel.

We build on the model developed by Jiménez [5] to derive the current-voltage characteristics by adding the effects of interface traps. The channel charge density is expressed as

$$n_{2D} = N_{2D}\ln(1+\alpha), \tag{1}$$

where

$$N_{2D} = \frac{g_s g_1 m_1^* kT}{2\pi\hbar^2} + \frac{g_s g_2 m_2^* kT}{2\pi\hbar^2}\mathrm{e}^{-\frac{\Delta E_{KQ}}{kT}},$$

$$\alpha = \mathrm{e}^{\frac{qV_C - E_0}{kT}},$$

where V_C is the voltage across C_q, q is the elementary charge, E_0 is half of the bandgap (E_g), which is 1.8 eV [8] for MoS_2. k is the Boltzmann constant and T is the temperature. h is the reduced planck constant. g_s is the spin degeneracy. g_1 and g_2 are the degeneracy of the K and Q conduction valleys, respectively. $m_1{}^*$ and $m_2{}^*$ are their respective DOS effective masses. For MoS_2, $g_s = 2$, $g_1 = 2$, $g_2 = 6$, $m_1{}^* = 0.48m_0$, and $m_2{}^* = 0.57m_0$ [8]. m_0 is the electron rest mass. ΔE_{KQ} is the energy separation between K and Q conduction valleys (∼0.11 eV for MoS_2 [8]).

The equivalent capacitive circuit of the MoS_2 FET is shown in Figure 1(b). C_{ox}, C_q, C_{it} represent the top oxide capacitance, quantum capacitance of the MoS_2 channel, and the capacitance owing to interface traps at the oxide-channel interface. V_T and V_n respectively are the threshold voltage and the channel potential of the MoS_2 FET. $C_{ox} = \varepsilon_{ox}/t_{ox}$, where ε_{ox} is the dielectric constant of the top gate oxide and t_{ox} is its thickness. C_q can be expressed as

$$C_q = q\frac{\mathrm{d}n_{2D}}{\mathrm{d}V_C} = \frac{q^2 N_{2D}\alpha}{(1+\alpha)kT}. \tag{2}$$

Figure 1(c) shows the schematic of V_{gs} dependences of C_{ox}, C_q, and C_{it}. The real C_{it} keeps as a constant in the sub-threshold region and becomes a complex function of V_{gs} when the FET goes into the transition and strong-inversion regions owing to the energy distribution of the interface traps [4]. That results in a large amount of numerical calculations in previous models [7,8]. On the other hand, according to experimental results [4], C_q increases exponentially

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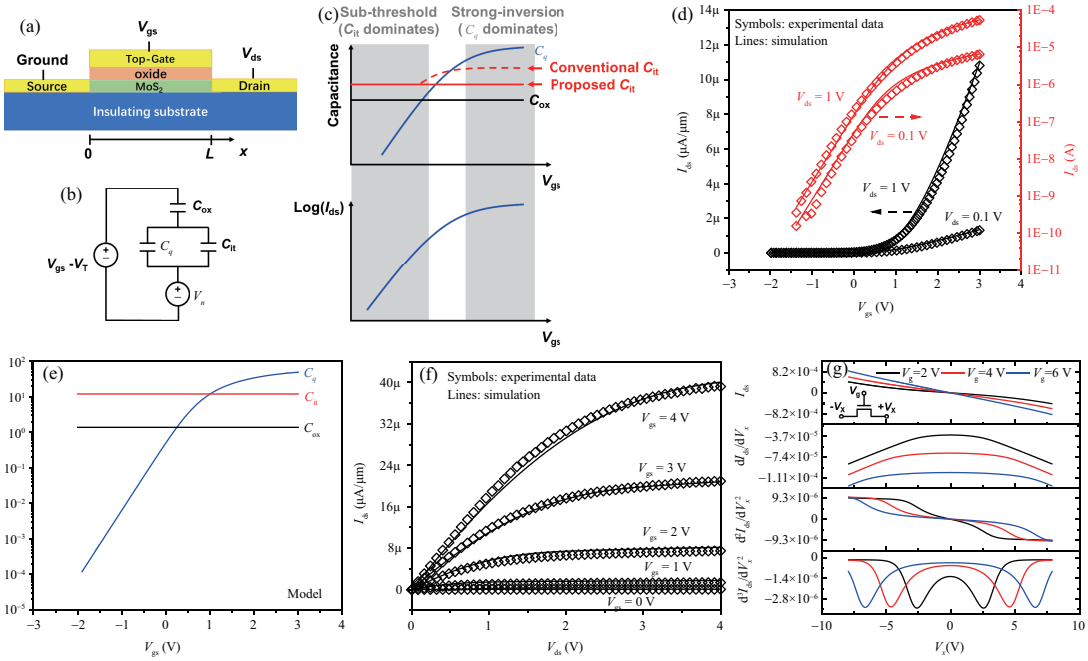

Figure 1 (Color online) (a) Schematic of a top-gate FET with a monolayer MoS_2 as its active channel. (b) Equivalent capacitive circuit of the MoS_2 FET. (c) Schematic of V_{gs} dependences of capacitances and I_{ds}. (d) Measured (symbol) and simulated (line) transfer characteristics. (e) Simulated V_{gs} dependence of capacitances. (f) Measured (symbol) and simulated (line) output characteristics. (g) Simulated Gummel symmetry test results.

with V_{gs} and thus C_{it} is negligible in the strong-inversion region. In the sub-threshold region, the sub-threshold swing (SS) is dominated by C_{it} and C_{ox}. Thus, it can be concluded that by extracting C_{it} in the sub-threshold region and taking it as a constant across all regions, the introduced error in the strong-inversion region is negligible. In this letter, C_{it} is assumed as

$$C_{it} = q^2 D_{it}, \tag{3}$$

where D_{it} is the density of interface traps.

At the position x in the channel, the bias potentials and capacitances are correlated with the channel charge (Q_n) as

$$(V_{gs} - V_T + V_n(x) - V_C(x))C_{ox} + (-C_{it}V_C(x) + Q_n(x)) = 0, \tag{4}$$

where $V_n(0) = 0$, $V_n(L) = V_{ds}$, $Q_n = -qn_{2D}$.

The current density J_D at the position x is expressed as

$$J_D(x) = Q_n(x)\mu\frac{\mathrm{d}V_n(x)}{\mathrm{d}x}, \tag{5}$$

where μ is the mobility.

By integrating J_D across all positions along the channel and changing the variable from x to V_n, the current I_D can be expressed as

$$I_D = \mu\frac{W}{L}\int_{V_{Cs}}^{V_{Cd}} Q_n\frac{\mathrm{d}V_n}{\mathrm{d}V_C}\mathrm{d}V_C. \tag{6}$$

where V_{Cs} and V_{Cd} respectively are the quantum potential at the source and drain. $\mathrm{d}V_n/\mathrm{d}V_C$ can be derived by differentiating (4) with respect to V_C.

Using all above equations, a simple analytical form of I_D is obtained:

$$I_D = \mu\frac{W}{L}\left\{\left(\frac{C_{ox}+C_{it}}{C_{ox}}\right)N_{2D}kT\alpha + \frac{q^2N_{2D}^2}{2C_{ox}}\ln^2(1+\alpha)\right\}_{V_{Cs}}^{V_{Cd}}. \tag{7}$$

The channel length modulation coefficient (λ) is additionally included as

$$I_{ds} = I_D(1 + \lambda V_{ds}). \tag{8}$$

The proposed compact model is validated using the experimental results. The device fabrication process [9] is described as follows. Monolayer MoS_2 film is first grown by chemical vapor deposition process on sapphire and then transferred onto the 30 nm Al_2O_3/doped silicon substrate. The channel is patterned using PMMA as mask and subsequently etched using CF_4 plasma. Source and drain electrodes are patterned by electron-beam lithography and 50 nm Au is deposited by E-beam evaporation. ML PTCDA and HfO_2 ($\varepsilon_{ox} = 14\varepsilon_0$, $t_{ox} = 9$ nm) are deposited onto the channel area. ε is the vacuum dielectric constant. The gate electrode (5 nm T_i/15 nm Au) is aligned to source and drain electrodes by the E-beam lithography. All electrical measurements are performed under a vacuum environment at room temperature (300 K).

Figure 1(d) shows the simulated (line) and experimental (symbols) transfer characteristics of the MoS_2 FET. Our model guarantees a good fit to the experimental results in both sub-threshold and strong-inversion regions with small deviations in the transition region. The deviation is mainly ascribed to that C_{it} is a function of V_g and is comparable with C_q in the transition region, whereas it is assumed as a constant in this model. However, as claimed in the introduction, the good fit in both sub-threshold and strong-inversion regions guarantees the application of this model in digital circuit design. In addition, only three fitting parameters — μ, V_T, and D_{it} — are required in the proposed model. The extracted $\mu = 1.2$ cm^2·V^{-1}·s^{-1}, $V_T = 1.1$ V. The extracted D_{it} is $\sim 6.6\times10^{13}$ cm^{-2}·e·V^{-1}, which is consistent

with other published data [4]. By optimizing the interface between MoS_2 channel and gate oxide, $D_{\rm it}$ can be reduced and μ can be improved.

The $V_{\rm gs}$ dependences of C_q, $C_{\rm ox}$, and $C_{\rm it}$ are shown in Figure 1(e). As is expected, $C_{\rm it}$ dominates in the sub-threshold region whereas C_q dominates in the strong-inversion region. The target frequency of this model is not high, that is the reason why the possible parasitic capacitances other than C_q, $C_{\rm ox}$, and $C_{\rm it}$ are neglected.

In addition to the transfer characteristics, a good fit to the output characteristics of the MoS_2 FET is shown in Figure 1(f). Our model also passes the Gummel symmetry test [7] results. As shown in Figure 1(g), $I_{\rm ds}$ and its even derivatives have odd symmetry around $V_x = 0$ V and odd derivatives have even symmetry around $V_x = 0$ V.

Conclusion. In this letter, we presented a compact model for TMD FETs considering the indispensable effects of interface traps. Different from the previous models where a large amount of numerical calculations are unavoidable, by simplifying the energy distribution of interface traps, we proposed a converging and accurate model that is validated by experimental results. Our model is suitable for efficient circuit explorations for future complex systems based on TMD FETs.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 61734003, 61521001, 61927808, 61851401).

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