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Layout dependence of total-ionizing-dose response in 65-nm bulk Si pMOSFET

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Dear editor,

Strain technology has become a common solution in the semiconductor manufacturing industry since 90-nm technology node to overcome the severe carrier mobility degradation of nanoscale microelectronic devices [1]. Since layout may affect the stress distribution, layout dependent effect (LDE) becomes a serious issue in advanced technology nodes.

Most previous works focus on the impact of LDE on time-zero device performance [1–3] and end-of-life (EOL) behaviors [4, 5]. Different layout design may lead to different device performance due to strain effect and pattern loading effects [3]. Moreover, the experimental results show that the bias temperature instability (BTI) and hot carrier injection (HCI) reliability are also layout dependent in nanoscale devices [4].

However, the impact of LDE on radiation effects is still unclear. Few papers focus on this issue. And limited research indicates that the radiation sensitivity of the devices is layout dependent. Rezzak et al. [6] firstly investigated the layout-related total ionizing dose (TID) response in 90-nm bulk Si NMOS devices, which shows that the radiation-induced leakage current increases with increasing gate-to-active area spacing, due to weaker compressive stress induced by shallow trench isolation (STI). For 45-nm strained SOI RF nFETs, different source/drain contact spacing and gate finger-to-gate finger spacing may result in the trade-offs between RF performance and TID degradation [7]. It is clear that the experimental research on LDE on radiation response of nanoscale device is quite limited and needs further research.

In this study, we experimentally demonstrate the layout dependence of TID response in 65-nm bulk Si pMOSFET for the first time. The results may deepen the understanding of the effect of strain on TID sensitivity of MOS devices and provide a guideline for the layout design of high performance and radiation-hardened IC.

Experiment. The devices used in the experiment are 65-nm low-threshold-voltage (LVT) core bulk silicon pMOSFETs fabricated by commercial 65-nm standard CMOS technology. Strain technology is adopted in the fabrication process. Different gate-to-active area spacing (SA) were specifically designed varying from 0.18 μm (default value) to 1 μm to investigate the effect of stress on the TID response. The definition of SA is shown in the inset of Figure 1(a). The device gate length (L) is 60 nm and the gate width (W) is 0.2 μm.

TID experiments were performed on a wafer-level TID platform at room temperature with a total dose up to 1 Mrad(Si) at Xinjiang Technical Institute of Physics and Chemistry (XTIPC), Chinese Academy of Sciences (CAS). The irradiation source was 60 keV X-ray with dose rate at 290.6 rad(Si)/s. All devices are unpackaged to avoid electro-static discharge (ESD) damage caused by packaging. During irradiation, the irradiation bias condition was ALL0 state (where all terminals grounded), which is reported as the 'worst-case' irradiation bias condition of planar bulk Si PMOS device [8, 9]. The in-situ I-V tests were performed immediately after irradiation using a probe card connected with switch mainframe and B1500A semiconductor device analyzer.

Results and discussion. For pMOSFETs, the strain technique aims to introduce compressive stress in the channel, thereby increasing hole mobility and improving device performance [1]. Therefore, the influence of different SA on the as-fabricated characteristics of the device is investigated first.

Figure 1(a) shows the box-plot of the drain current of PMOS devices with different SA values at the same gate overdrive voltage ($\boldsymbol{V}_{\rm ov}$ = 0.6 V). Considering device performance fluctuation, 20 fresh samples were tested to obtain statistical results. It can be seen from the figure that as SA increases, the overdrive current increases. Compared to devices with 0.18 μm SA, the average overdrive current of devices with 1 μm SA is 8% larger. This is attributed to the fact that the increase in SA leads to an increase in the volume of the source and drain regions, larger compressive stress is introduced in the channel, resulting in larger hole mobility and overdrive current.

Then, typical degradation behavior of the electrical char-

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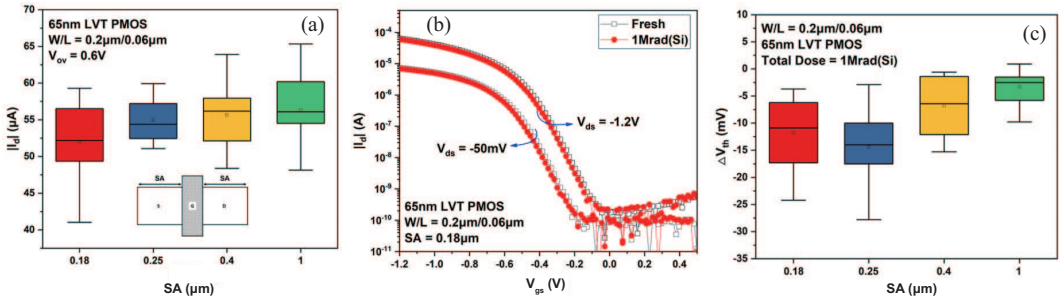

Figure 1 (Color online) (a) Box-plot of the drain current of PMOS devices as a function of SA values at the same overdrive voltage ($\boldsymbol{V}_{\rm ov}$ = 0.6 V). The inset shows the definition of SA. (b) The typical transfer characteristic curves of 65-nm PMOS device with SA of 0.18 μm before and after irradiation. (c) Box-plot of $\boldsymbol{V}_{\rm th}$ shift as a function of SA values after 1 Mrad(Si) TID irradiation.

acteristics of 65-nm pMOSFET after X-ray irradiation is demonstrated. Figure 1(b) shows the typical transfer characteristic curves of 65-nm PMOS device with SA of 0.18 μm before and after irradiation. It can be seen from the figure that after 1 Mrad(Si) TID irradiation, the threshold voltage ($\boldsymbol{V}_{\rm th}$) shows a negative shift of 16 mV, and the on-state current ($\boldsymbol{I}_{\rm on}$) decreases by about 6.3%. This degradation is due to the irradiation-induced trapped charges in STI [9]. These trapped charges affect the channel potential, pull down the channel energy band and result in negative $\boldsymbol{V}_{\rm th}$ shift. The increase in the absolute value of threshold voltage results in the decrease of $\boldsymbol{I}_{\rm on}$. In addition, the off-state leakage current ($\boldsymbol{I}_{\rm off}$) of the devices is barely changed, which is attributed to the N-type doped body region. The positive trapped charges in STI cannot form a parasitic leakage path that connects the source and drain.

Finally, the layout dependence of TID response in 65-nm bulk Si pMOSFET is investigated. Figure 1(c) shows the box-plot of $\boldsymbol{V}_{\rm th}$ shift as a function of SA values after 1 Mrad(Si) TID irradiation. Each SA contains test results of 11-15 irradiated samples. It can be seen from the figure that with SA decreasing, the $\boldsymbol{V}_{\rm th}$ shift increases. For devices with SA of 0.18 μm and 0.25 μm, the average $\boldsymbol{V}_{\rm th}$ shift is 12-15 mV, while for devices with SA of 1 μm, the average $\boldsymbol{V}_{\rm th}$ shift is less than 5 mV, which is reduced by more than 50%. Therefore, increasing SA may enhance radiation-hardness of 65-nm PMOS devices.

The main cause of the layout dependence of TID response is the difference in the stress distribution in the channel. It is known that increasing SA induces the enhanced compressive stress in the channel. On one hand, the change in stress causes different distribution of impurities in the channel [6], which affects the modulation of the channel potential by the trapped charges in STI. On the other hand, different channel stress may affect the interface characteristics of gate oxide and channel. Specifically, for short SA devices, smaller compressive stress will cause the energy level splitting of the heavy hole (HH) band and the light hole (LH) band of the valence band to decrease, which reduces the hole trapping barrier and makes it easier to trap holes near the gate oxide/channel interface [4]. Therefore, for 65-nm PMOS devices, increasing SA is not only beneficial to improve the device performance, but also helpful to reduce the TID sensitivity of the device, which may provide a guideline for both enhanced performance and better radiation-hardness of IC layout design. It should be noted that after the SA increases to a certain value (0.4 μm), $\boldsymbol{V}_{\rm th}$ shift is basically saturated, so from the perspective of radiation, it just needs to select a suitable SA value.

Conclusion. In summary, the layout dependence of TID response in 65-nm bulk Si pMOSFETs is firstly experimentally demonstrated in this work. As SA increases from 0.18 to 1 μm, the average overdrive current increases about 8%, which is attributed to larger compressive stress in the channel. After 1 Mrad(Si) TID irradiation, the average irradiation-induced $\boldsymbol{V}_{\rm th}$ shift of devices with SA of 1 μm is reduced by more than 50% compared to devices with SA of 0.18 and 0.25 μm. This is attributed to the impact of channel stress on the impurity distribution and interface characteristics between gate oxide and channel. Based on the experimental results, increasing SA is beneficial to improve both the performance and the radiation-hardness of 65-nm PMOS devices, which may provide guideline for the layout design of aerospace application ICs.

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