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A 530 nA quiescent current low-dropout regulator with embedded reference for wake-up receivers

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Dear editor,

Low power transceivers are essential in the wireless personal area network (WPAN) applications [1]. To reduce transceivers' power in standby mode, wake-up receivers (WuRx's) are now widely used in WPAN applications [2]. Those WuRx's are always-on in the system and are usually powered by batteries. A compact low-dropout (LDO) voltage regulator with very small quiescent current is required to convert the battery voltage to the desired working voltage.

Some recently reported low quiescent current LDOs are digital LDOs or the quasi-digital LDOs [3], but they exhibit very poor power supply rejection ratio (PSR) or large output ripple. For WuRx's which are sensitive to the power supply noise/disturbance, an analog LDO is preferred. However, analog LDOs usually need a large decoupling capacitor, such as the analog LDO presented in [4] requires a 240 pF decoupling capacitor under the light load condition. Nevertheless, most LDOs need a separate voltage reference which requires extra current and chip area. The analog LDO with an embedded voltage reference in [5] consumes very low quiescent current (110 nA). However, it could only output a voltage around 1.2 V.

In this study, a low quiescent current LDO with an embedded voltage reference is proposed. An error amplifier (EA) with asymmetrical input transistors is used for the closed-loop voltage regulation. The EA's input transistor pair is biased in the moderate inversion region, instead of the commonly used weak inversion region. The LDO output range is expanded without extra power consumption. The chip is designed and fabricated in a 180 nm CMOS process. The output voltage can be expanded to a given value between 1.3 V and 1.8 V with different settings of design parameters. The maximum quiescent current is only 530 nA, with a 1.6 V output and an input range of 1.8–3.7 V. The load current range is 0–100 μA.

Circuit architecture. The circuit architecture of the proposed LDO regulator is shown in Figure 1(a). The core circuitry consists of an EA with asymmetrical input transistors, a PMOS source follower buffer, a PMOS power passing transistor M_{pass}, a feedback network, and a Miller compensation network. There is no extra reference circuit required for this LDO. The auxiliary circuitry includes an adaptive biasing circuit for fast transient response. All the transistors used in this LDO are thick gate-oxide devices to tolerate possible high battery voltage up to 3.7 V. The LDO regulator has an embedded voltage reference which is similar to that in [5]. However, the structure in [5] could only output the bandgap voltage of ∼1.2 V. In this study, the output voltage is greatly expanded.

Voltage regulation with embedded reference. If the EA's input transistors M_1 and M_2 are biased in the weak inversion region as [5], the drain-source current I_D and the gate-source voltage V_{GS_WI}

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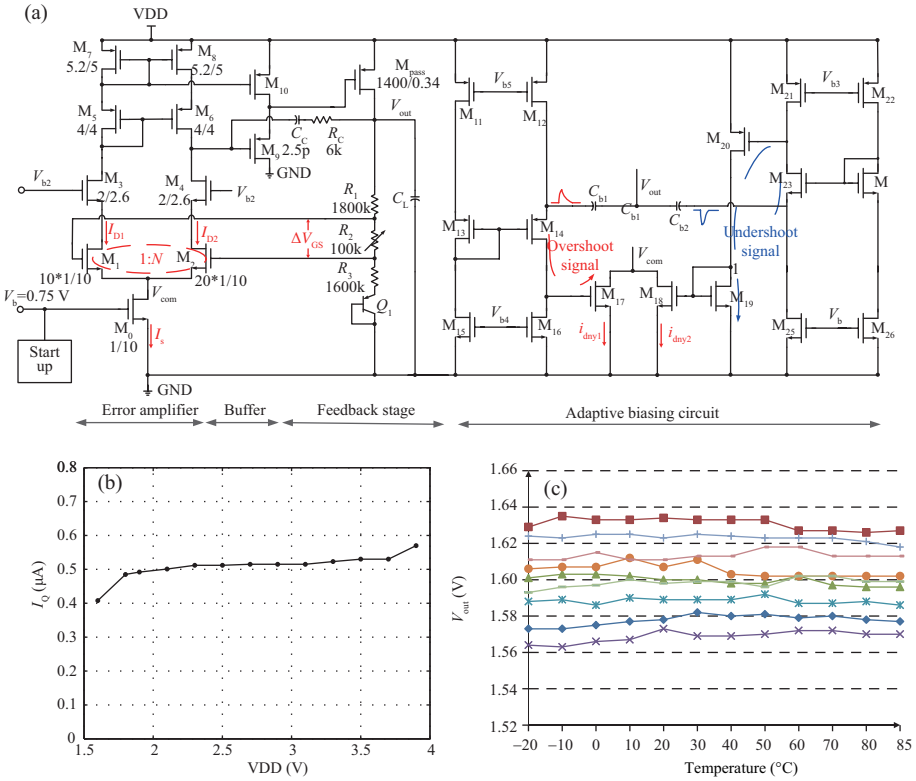

Figure 1 (Color online) (a) Core circuit of the proposed LDO regulator (biasing circuit not included); (b) measured quiescent current with 100 μA current load; (c) measured output voltages of 9 samples across −20°C – +85°C temperature range.

have a relationship [6] given by

$$V_{\mathrm{GS\_WI}} = \frac{nkT}{q} \ln \frac{I_{\mathrm{D}}}{I_{\mathrm{D0}}} \frac{1}{W/L}, \tag{1}$$

where I_{D0} is the current density of a MOSFET in weak inversion region, W and L refer to the size of a MOSFET, k is the Boltzmann factor, q is the charge of an electron, T is the absolute temperature, and n is a process related parameter. With the well matched cascode current mirror formed by $\mathrm{M_5}$–$\mathrm{M_8}$ as the load, $\mathrm{M_1}$ and $\mathrm{M_2}$ have the same current. In this design, $\mathrm{M_1}$ and $\mathrm{M_2}$ have the same channel length and different channel width ($W_2/W_1 = N$), which results in unequal $V_{\mathrm{GS\_WI}}$. Considering the input transistor threshold voltage mismatch, the difference of $V_{\mathrm{GS\_WI}}$ is

$$\Delta V_{\mathrm{GS\_WI}} = \frac{nkT}{q} \ln N + \Delta V_{\mathrm{T}}. \tag{2}$$

It can be concluded from (2) that $\Delta V_{\mathrm{GS\_WI}}$ contains the PTAT component and the constant component. We can rewrite it as

$$\Delta V_{\mathrm{GS\_WI}} = A \cdot T + \Delta V_{\mathrm{T}}, \text{ where } A = \frac{nk}{q} \ln N. \tag{3}$$

On the other hand, if $\mathrm{M_1}$ and $\mathrm{M_2}$ are biased in the strong inversion region, we have

$$V_{\mathrm{GS\_SI}} = V_{\mathrm{T}} + (V_{\mathrm{b}} - V_{\mathrm{T}}) \sqrt{\frac{W_0/L_0}{2W_{1,2}/L}}, \tag{4}$$

where V_{T} is the transistor threshold voltage, and V_{b} is the gate voltage of the tail current transistor $\mathrm{M_0}$, respectively. $I_{\mathrm{S}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W_0}{L_0} (V_{\mathrm{b}} - V_{\mathrm{T}})^2$ is actually the tail current through $\mathrm{M_0}$. $\mathrm{M_1}$ and $\mathrm{M_2}$ have the same biasing current equal to $I_{\mathrm{S}}/2$. Considering the input transistor threshold mismatch, the V_{GS} difference of $\mathrm{M_1}$ and $\mathrm{M_2}$ in this region is given by

$$\Delta V_{\mathrm{GS\_SI}} = C + \Delta V_{\mathrm{T}}, \tag{5}$$

where $C = \sqrt{\frac{1}{2}\frac{W_0 L}{W_1 L_0}} (V_{\mathrm{b}} - V_{\mathrm{T}})(1 - \frac{1}{\sqrt{N}})$ and it is treated as a constant.

In this design, $\mathrm{M_1}$ and $\mathrm{M_2}$ are biased in the moderate inversion region, i.e., between the weak inversion region and the strong inversion region. The drain current of $\mathrm{M_1}/\mathrm{M_2}$ consists of both the drift and the diffusion components. Roughly speaking, ΔV_{GS} can be decomposed into two components, namely, the part described by (3), and the part described by (5).

$$\Delta V_{\mathrm{GS}} \approx \alpha A T + \beta C + \alpha \Delta V_{\mathrm{T}} + \beta \Delta V_{\mathrm{T}}. \tag{6}$$

It is not easy to get the analytical solutions for the coefficients α and β in (6), but their values can be found using the transistor-level simulation. With the feedback loop, the LDO output voltage is given by

$$V_{\rm OUT} = V_{\rm BE} + F\Delta V_{\rm GS}, \tag{7}$$

in which $V_{\rm BE}$ is the base-emitter voltage of the BJT Q_1 in Figure 1(a), and $F{=}(R_1{+}R_2{+}R_3)/R_2$. According to [7], $V_{\rm BE}$ has a negative temperature coefficient (temp-co), and it can be denoted as

$$V_{\rm BE} \approx V_{\rm G0} - B \cdot T, \tag{8}$$

where $V_{\rm G0}$ is a constant and $-B$ is the temp-co of $V_{\rm BE}$.

Combining (6)–(8) leads to

$$V_{\rm OUT} \approx (\alpha FA - B)T + V_{\rm G0} + \beta F\sqrt{\frac{1}{2}\frac{W_0L}{W_1L_0}}(V_{\rm b} - V_{\rm T}) \cdot \left(1 - \frac{1}{\sqrt{N}}\right) + F(\alpha\Delta V_{\rm T} + \beta\Delta V_{\rm T}). \tag{9}$$

Eq. (9) consists of three parts, namely, the constant part, the temperature dependent part and the part caused by process variation. The values of F, α and β can be adjusted by changing R_2, N and $V_{\rm b}$. Although it is impractical to find the analytical solution for R_2, N and $V_{\rm b}$, Eq. (9) clearly shows the feasibility to obtain $V_{\rm OUT}$ with the desired nominal voltage and a zero temp-co. In the real design, the transistor-level simulation is used to find the appropriate values of R_2, N and $V_{\rm b}$. The final chosen components' values are marked on Figure 1(a). After fabrication, the values of R_2 and $V_{\rm b}$ can be tuned by programming the on-chip control switches. More design details are included in Appendixes A–D.

Experimental results. The proposed LDO has been fabricated in a 180 nm CMOS technology. It occupies an active area of 0.11 $\rm mm^2$ (270 μm × 410 μm) excluding the bonding pads. Figure 1(b) shows the measured quiescent current with different input voltages. The maximum quiescent current is 530 nA between 1.8 V and 3.7 V input range.

Nine samples randomly selected from the fabricated chips are measured to validate the temperature independence. For each chip measured, the resistor R_2 and the biasing voltage $V_{\rm b}$ are iterated to find the proper settings, which makes the output voltage close to 1.6 V and the temp-co flat at the room temperature. Figure 1(c) shows measured output voltages of 9 LDOs within temperature range of −20°C – +85°C. The average voltage is 1.601 V and the standard variance is 19.1 mV, which means ±3.58% 3σ inaccuracy. More experimental results are included in Appendix E.

Conclusion. A 530 nA quiescent current LDO regulator with the embedded voltage reference is presented. The error amplifier transistors are biased in the moderate inversion region instead of the commonly used weak inversion region to expand the output voltage range. The LDO output voltage is 1.6 V with an input voltage ranges between 1.8 V and 3.7 V. It is stable for the load current range of 0–100 μA. With the low quiescent current, wide input range and small chip area, the proposed LDO is suitable for integration in ultra-low power WPAN SoCs powered by miniature batteries.

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Supporting information Appendixes A–E. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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