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• **Supplementary File** •

A 530nA quiescent current low-dropout regulator with embedded reference for wake-up receivers

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Appendix A Biasing voltage generation circuit

Figure A1 shows the biasing voltage generation circuit. M_{27}-M_{30} and R_4 form a circuit to generate the supply-independent biasing voltage V_b. M_{29} works in the saturation region, and V_b can be calculated from the following equation

$$\frac{1}{2}\mu_n C_{ox}\frac{W_{29}}{L_{29}}(V_b - V_{T29})^2 = \frac{V_b}{R_4}. \tag{A1}$$

V_b is determined by the size of M_{29} and the resistor R_4. After fabrication, V_b can be adjusted by tuning R_4. At the typical device corner, the biasing circuit consumes about 85 nA current in simulation.

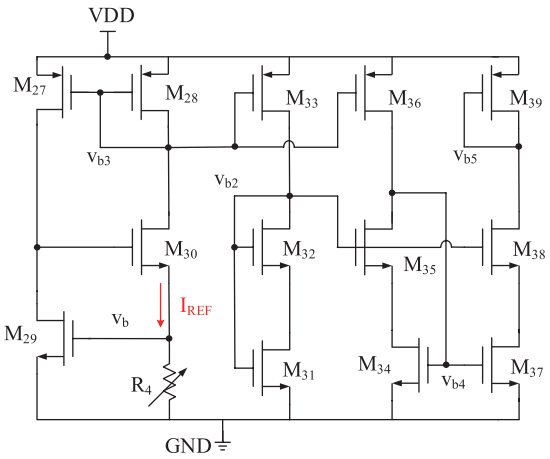

Figure A1 Biasing voltage generation circuit.

The biasing voltage V_b has a negative temperature coefficient (temp-co). This fact actually contributes a negative temp-co component to ΔV_{GS_SI}. This negative temp-co effect is about 1/6 of the positive temp-co of the PTAT component. In this design, the PTAT component needs to be adjusted to neutralize all the negative temperature coefficients contributed by other circuit blocks including the V_b generation circuit.

Appendix B Output voltage regulation

According to the analysis in this article, the output of the LDO regulator can be denoted as

$$V_{OUT} \approx (\alpha FA - B)T + V_{G0} + \beta F\sqrt{\frac{1}{2}\frac{W_0 L}{W_1 L_0}}(V_b - V_T)\cdot(1 - \frac{1}{\sqrt{N}}) + F(\alpha\Delta V_T + \beta\Delta V_T). \tag{B1}$$

Eq. (B1) shows that the nominal output and the temp-co can be adjusted by tuning F and V_b. Actually F is tuned by changing the resistor R_2 and V_b is tuned by changing the resistor R_4. After the chip fabrication, the values of R_2 and R_4 can be tuned by programming the on-chip control switches.

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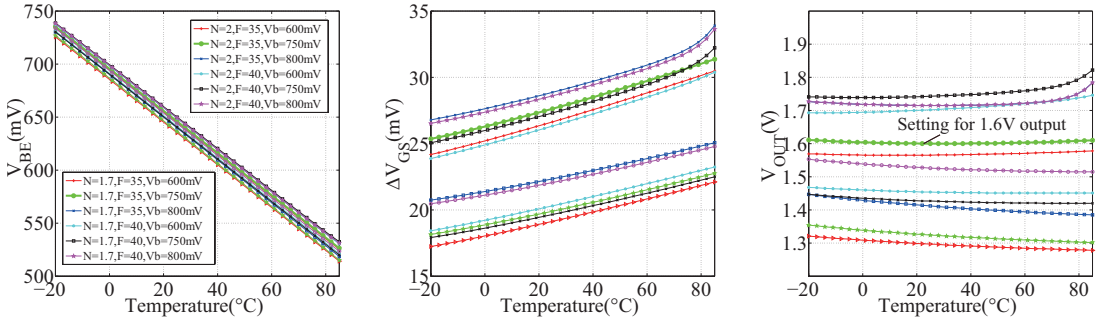


Figure B1 $V_{\rm BE}$, $\Delta V_{\rm GS}$, $V_{\rm OUT}$ vs. temperature with different circuit settings. The supply voltage is 3.7 V.

In the design phase, the transistor-level simulation is used to find the appropriate values of R_2, N and $V_{\rm b}$. Figure B1 shows $\Delta V_{\rm GS}$, $V_{\rm BE}$, and $V_{\rm OUT}$ with respect to the temperature under different settings of N, F and $V_{\rm b}$. It is shown that the presented LDO can provide a wide output range from 1.3 V to 1.8 V, by changing the parameters N, R_2 and $V_{\rm b}$. In this work, the target is to obtain a 1.6 V output with zero temp-co. The setting of parameters is finally determined as N=2, F=35, and $V_{\rm b}$ =0.75 V through simulation, which makes the constant part close to 1.6 V, and the temp-co close to 0. Different $\rm R_2$ and $\rm R_4$ settings are iterated to find the optimal $\rm R_2$ and $\rm R_4$ that exactly give the desired nominal output and zero temp-co. The iteration easily converges during the design phase. Considering that $\rm R_2$ and $\rm R_4$ may deviate from the design values due to the process variation, both $\rm R_2$ and $\rm R_4$ have a trimming range ±20%. The presented chip has 8 trimming bits, with each 4 bits for $\rm R_2$ and $\rm R_4$ correspondingly. Note that $\rm R_2$ and $\rm R_4$ have limited trimming resolution, it is not guaranteed that the desired voltage and zero temp-co are always exactly achievable. However, after trimming, the output voltage error can be reduced to less than 5%, and the temp-co can be reduced to no more than 60 ppm/°C.

After the chip fabrication, $\rm R_2$ and $\rm R_4$ need to be tuned to compensate for the chip-to-chip variation. Since $\rm R_2$ and $\rm R_4$ have 8 trimming bits in total, there are only 256 voltage-temperature curves. For the cost-insensitive applications, all the 256 voltage-temperature curves can be measured for each individual LDO, and then the trimming setting that gives the acceptable voltage error and temperature coefficient will be chosen and saved as the calibration setting. For the cost-sensitive applications, the trimming code can be found based on a few selected LDO chips, and then applied to all the other LDO chips from the same lot.

It can be concluded from (B1) that the variation in the biasing voltage $V_{\rm b}$ and the input transistor mismatch in the error amplifier (EA) will introduce an offset in the LDO output voltage. With the chosen devices' sizes, namely, W_0/L_0 =1/10 , W_1/L_1 =10/10, F=35 and N=2, the coefficient of ($V_{\rm b}$-$V_{\rm T}$) in (B1) can be calculated as 2.3β. Here, β is a coefficient less than 1. Roughly, if $V_{\rm b}$ varies by 50 mV due to the process variation, there will be about the same amount of offset in the LDO output voltage. On the other hand, the mismatch error in the input transistor will be amplified by F=35 times toward the LDO output voltage. Although the EA's input transistors are carefully sized to reduce the threshold voltage mismatch error to about 1 mV, this mismatch error will cause about 35 mV offset in the LDO output. The total output offset error will be summed to about 100 mV with all the variations considered.

The Monte-Carlo simulation has been performed to check the output voltage variation with process variation. Figure B2 shows the simulated output voltages distribution from the Monte-Carlo simulation. The average output value is 1.596 V and the standard deviation is 101.24 mV. The simulated voltage variation matches the measured results.

It is very critical to have the input transistors bias in the moderate inversion region so that (B1) is valid. In this design, the typical tail current through $\rm M_0$ is 120 nA, and the process-voltage-temperature (PVT) simulations show that the actual tail current varies from 95 nA to 176 nA. The tail current is evenly divided between the input transistors $\rm M_1$ and $\rm M_2$ in the error amplifier, which means $I_{\rm DS}$ of $\rm M_1$ and $\rm M_2$ varies from 47.5 nA to 88 nA. $\rm M_1$ and $\rm M_2$ have different W/L ratios, and consequently different boundaries between the weak and strong inversion. The drain-source current boundaries of $I_{\rm DSt1}$ and $I_{\rm DSt2}$ are 0.23 μA and 0.46 μA, respectively, based on the equation [1]

$$I_{\rm DSt} = 2n\mu_{\rm n}C_{\rm ox}\frac{W}{L}(\frac{kT}{q})^2 \tag{B2}$$

The inversion coefficient ($i_{\rm c}$=$I_{\rm DS}/I_{\rm DSt}$) variation range of $\rm M_1$ and $\rm M_2$ is calculated as 0.21-0.38 and 0.105-0.19, respectively. The moderate inversion region is that $i_{\rm c}$ ranges between 0.1 and 10 [1]. This means that both input transistors of the error amplifier are guaranteed to work in the moderate inversion region, even with the PVT variations.

Appendix C Adaptive biasing circuit

The LDOs with very low quiescent current usually have limited biasing current budgets for the error amplifier, which may lead to slow transient response. The adaptive biasing techniques [2–4] were proposed to increase the biasing current at the transient instant without increasing the power dissipation in the steady state. A dynamically-biased shunt feedback was used at the buffer stage in [2]. The biasing current of the buffer could be increased according to the magnitude of the output current. In [3], an adaptive-biasing voltage buffer was used both for the frequency compensation and the slew rate

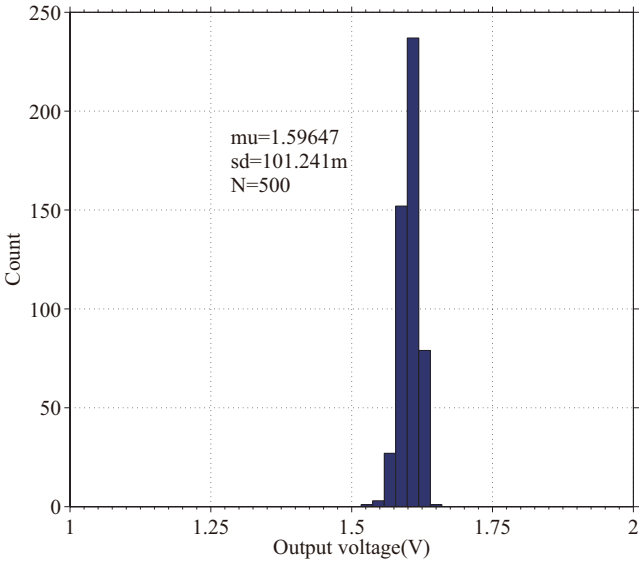


Figure B2 Output voltage distribution from 500 MC simulation.

enhancement. The adaptive biasing technique in [4] used a sensing transistor parallel to the pass transistor to sense the current of the pass transistor. A load dependent transient current will be generated when the load changes.

In this work, the adaptive biasing technique has also been used to improve the transient response. The adaptive biasing circuit adopts the voltage detector in [5] to sense the output voltage variation. Once the output voltage over/undershoot is detected, the dynamic biasing current is generated to enhance the EA temporarily.

When an overshoot occurs, the overshoot spike is detected by C_{b1} and then amplified by M_{14} and M_{17}. A dynamic current i_{dyn1} is generated and added to the EA through M_{17}. The current i_{dyn1} increases the bandwidth of the EA which improves the transient response of the LDO regulator. In the normal work condition, M_{17} is in the cut-off region and no extra current is consumed.

Similarly, when an undershoot occurs, the undershoot dip is detected by C_{b2} and then amplified by M_{23} and M_{20}. Another dynamic current i_{dyn2} is generated and added to the EA through M_{18}. The adaptive biasing circuit consumes less than 40 nA quiescent current and provides 1 μA dynamic current lasting for 10 μs in both the undershoot and the overshoot situation.

The overshoot and undershoot detection circuit forms two extra feedback loop and the stability issue needs to be considered. In this design, the phase margin of these two feedback loops have been simulated with the PVT variations. The overshoot and undershoot detection feedback loops exhibit minimal phase marge of 44° and 37°, respectively. Both loops are stable with the PVT variations.

Appendix D Stability and frequency compensation

The presented LDO requires no external capacitor. The open loop small-signal ac model of the regulator is shown in Figure D1. In Figure D1, g_{m1} is the transconductance of the EA and r_{o1} refers to the output resistance of the EA. g_{mp} is the transconductance of the PMOS pass transistor. "1" stands for the source follower buffer. C_L refers to the on-chip decoupling capacitor. R_C is the resistor in series with the Miller capacitor C_C. R_L refers to the shunt resistance of M_{pass} output resistance, the load and the feedback resistors. The gate capacitor of M_{pass} is large and a dominant pole may occur in the gate of M_{pass}. The source follower buffer is used to push this pole to high frequency. The pole due to the gate capacitor of M_{pass} has been carefully checked. In this design, under the typical device corner with 100 μA load current, the pass transistor M_{pass} has the following parameters: C_{gd}=550 fF, g_m=2.1 mS, r_{ds}=15.65 kΩ which are obtained through simulation. With the Miller effect, M_{pass} has an equivalent input capacitance as given by $g_m r_{ds} C_{gd}$=18 pF. To push the parasitic pole due to the gate capacitor of M_{pass} to the high frequency, a source follower buffer with large g_m is used. In this design, the typical transconductance of the buffer transistor M_9 is about 62 μS with the careful bias setting. Then the frequency of the parasitic pole p_3 is about 540 kHz. Note that the gain bandwidth product (GBW) of this LDO is about 120 kHz under the typical corner, and the non-dominant pole p_{nd} is about 300 kHz, the extra pole p_3 does not hurt the overall phase margin much.

The LDO has two poles of concern, namely, the pole at the EA output node and the pole at the LDO output node. The open loop transfer function of the small-signal model can be denoted as

$$A_v = -\frac{g_m g_{mp} R_L r_{o1}[1 - sC_C(g_{mp}^{-1} - R_C)]}{s^2 C_L C_C R_L (r_{o1} + R_C) + s(g_{mp} C_C R_L r_{o1} + C_L R_L + C_C R_C + C_C R_L + C_C r_{o1}) + 1}. \quad \text{(D1)}$$

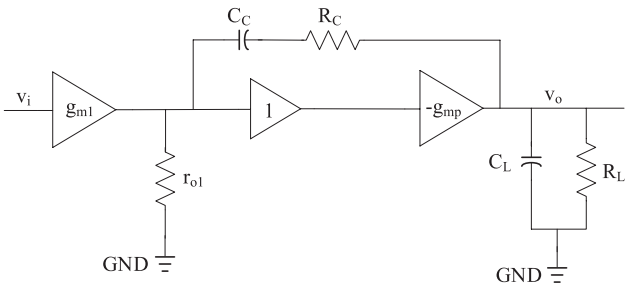


Figure D1 Open loop small-signal ac model of the proposed LDO regulator.

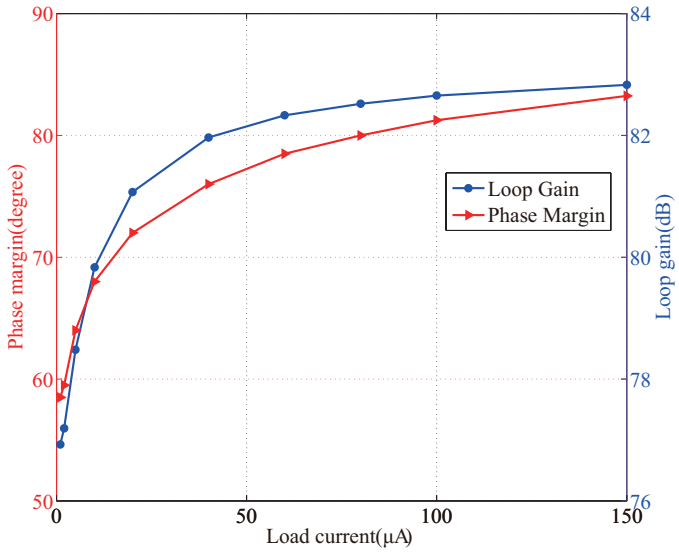


Figure D2 Simulated loop gain and phase of the proposed LDO with different load currents.

In this design, $g_{\rm mp}r_{\rm o1}C_{\rm C}$ is greater than $C_{\rm L}$ in all load conditions. The dominant pole lies in the output node of the EA, which is due to the effect of Miller capacitor. A non-dominant pole lies in the output node of the LDO regulator. Because of Miller compensation, the dominant pole $p_{\rm d}$ and the non-dominant pole $p_{\rm nd}$ are separated far apart. From (D1), the poles and zeros can be concluded as follows.

$$p_{\rm d} = -\frac{1}{2\pi g_{\rm mp}C_{\rm C}R_{\rm L}r_{\rm o1}}. \tag{D2}$$

$$p_{\rm nd} = -\frac{g_{\rm mp}r_{\rm o1}}{2\pi C_{\rm L}(r_{\rm o1}+R_{\rm C})}. \tag{D3}$$

$$z = \frac{g_{\rm mp}}{2\pi C_{\rm C}(1-g_{\rm mp}R_{\rm C})}. \tag{D4}$$

The Miller compensation produces a zero whose polarity depends on the relation between $\rm R_C$ and $1/g_{\rm mp}$. When $\rm R_C$ is greater than $1/g_{\rm mp}$, the zero is negative, which can be used to cancel a pole. In this design, $p_{\rm nd}$ given by (D3) is almost equal to z given by (D4) for the maximum load current of 100 μA, which leads to the pole-zero cancellation. When the load current is 0 μA, the transconductance of the PMOS pass transistor $\rm M_{pass}$ decreases and the non-dominant pole $p_{\rm nd}$ splits from the zero z. However, a phase margin of 55° is still guaranteed in the zero load condition. The simulated loop gain and phase margin with different current loads are shown in Figure D2, which verifies the stability of the LDO when the load is between 0 and 100 μA.

Appendix E Experimental results

The proposed LDO regulator has been designed and fabricated in a 180 nm CMOS process. Figure E1 shows the layout and microphotograph of the LDO regulator. It occupies an active area of 0.11 $\rm mm^2$ (270 μm * 410 μm) excluding the bonding pads. The load current can vary from 0 to 100 μA while the LDO regulator maintains stable. An on-chip load capacitor of 30 pF and a Miller capacitor of 2.5 pF are used for stability compensation. No off-chip capacitor is required. The maximum quiescent current is 530 nA with 1.8 V to 3.7 V input range and 1.6 V output under all load conditions.

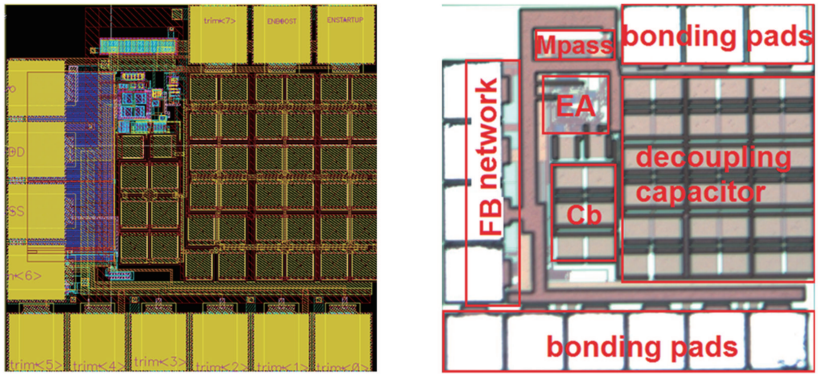
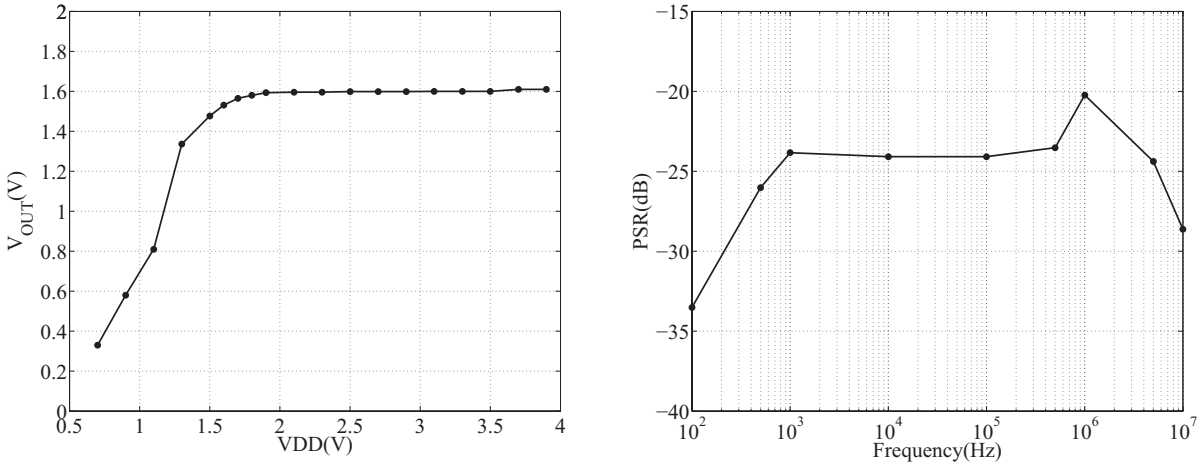
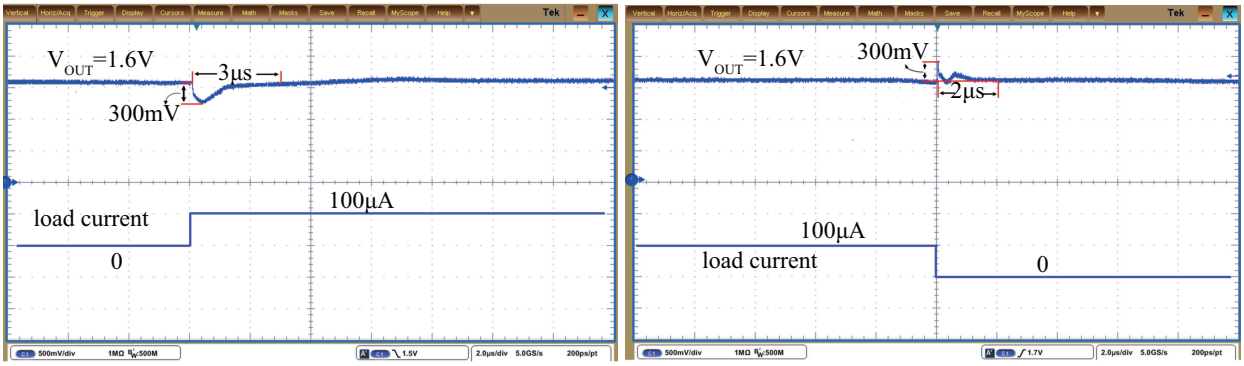


Figure E1 Layout and microphotograph of the proposed LDO regulator.



(a) (b)

Figure E2 (a) Measured line regulation with 100 μA current load. (b) Measured PSR with 100 μA current load and 3.7 V input.



(a) (b)

Figure E3 Measured load transient response with 100 μA load current. (a) Undershoot scene. (b) Overshoot scene.

The measured line regulation is shown in Figure E2(a). The drop-out voltage is about 200 mV and the line regulation is 1.6 mV/V. The PSR is measured with a function generator and an oscilloscope. The measured PSR with 100 μA load current and 3.7 V input voltage is shown in Figure E2(b). The worst PSR is at the frequency of 1 MHz, which is about -20 dB.

Figure E3 shows the measured load transient response. The load current is switched between 0 and 100 μA with 1 ns rising and falling time in this measurement. With the aid of the adaptive biasing circuit, the LDO can settle down in less than 3 μs when the voltage overshoot/undershoot happens.

In Table E1, the proposed low-power LDO performance is summarized and compared to the state-of-the-art light load LDOs. To make the comparison, the figure-of-merit (FOM) proposed in [6], as shown in (E1), is adopted in this paper.

$$FOM = (I_{\rm Q}/I_{\rm load}) \times (V_{\rm droop}/V_{\rm OUT}) \times C_{\rm out}. \tag{E1}$$

In (E1), $V_{\rm droop}$ refers to the undershoot voltage and $C_{\rm out}$ is the output decoupling capacitor. The smaller the FOM is, the better the design is. Among all the listed works, this work achieves the best FOM.

Table E1 Performance summary and comparison

Parameters	[6]	[7]	[8]	[9]	[10]	[11]	This work
Technology(nm)	65	65	130	65	65	150	180
Area without Cap.(mm^2)	0.029	0.0023	0.0012	0.087	0.023*	N/A	0.029
Decoupling Cap.(F)	400p	400p	200n	240p	130p	250p	30p
Power Supply(V)	0.5-1	0.5-1	1.9-3.3	1.2	1.15-1.2	1.4-2.2	1.8-3.7
Load Current(μA)	7.2-3511	0.1-2000	0-100	100-25000	1000	0.1-25	0-100
Output Voltage(V)	0.45-0.95	0.3-0.45	1.8	1	1	1.25	1.6
Dropout (mV)	50	50	100	200	150	150	200
Undershoot(mV)	40	40	47*	225	43	200**	300
Line Regulation(mv/V)	N/A	2.3	N/A	3.8	37.1	N/A	1.6
Quiescent Current (μA)	12.5-216	14	0.98-12.5	8-297.5	50-90	0.11	0.48-0.53
PSR@10kHz(dB)	N/A	N/A	N/A	-70	-22	N/A	-24
Settling time(μs)	80	0.1	N/A	1.5	0.2	N/A	3
Voltage Reference	Ext.	Ext.	Ext.	Ext.	Ext.	Int.	Int.
FOM(pF)	1.11	0.249	51.18	0.64	0.28	0.176	0.03

*Output voltage ripple.
**Area including capacitor.

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