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Single-event-transient effects in silicon-on-insulator ferroelectric double-gate vertical tunneling field effect transistors

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Dear editor,

Ferroelectric tunneling FETs (FeTFETs) are the increasingly significant research topics on novel low-power electronic devices [1, 2], because ferroelectric materials' negative capacitance effect is helpful to boost the channel potential and increase the on-state current in TFETs. Ferroelectric materials show radiation hard performance against radiation, which is helpful for devices based on this type of material utilized in harsh environment [3, 4]. Single-event-transient (SET) effects are caused by high energy particles in space or terrestrial radiation environment, which may increase the probability of soft-error or even lead to catastrophic accidents in the spacecraft [5, 6]. Research on the irradiation effects of FeTFETs under heavy ion strike is therefore extremely important to evaluate use of these devices for potential missions in space environments. In order to boost the devices' performance, we propose a new silicon-on-insulator double-gate FeTFET (SOI DG-FeTFET) with the Si:HfO_2 ferroelectric gate dielectric. The single-event-transient effects in SOI DG-FeTFET were investigated using a synopsys sentaurus technology computer aided design (TCAD) simulator [7].

Device structure and simulation setup. The two-dimensional (2D) architecture of the SOI DG-FeTFET considered in the simulation is shown in Figure 1(a). In this structure, 10 nm thick Si:HfO_2 ferroelectric layer is used as the gate dielectric, and amorphous HfO_2 film with 2 nm thickness is used as a gate insulator between the poly-crystalline Si:HfO_2 layer and Si substrate. The detailed geometry parameters for SOI DG-FeTFET are given in Figure 1(b). Complete device structure was built in the simulation, with left and right drains part of the same node. Because the structure is symmetrical, the right half of the device is chosen as the incident position of heavy ions. Ions strike in the middle of the body in the right half of the device with linear energy transfer (LET) ranges from 10 to 100 MeV·cm^2/mg. Collection charge in the complete device structure is taken into consideration. The ion trajectories have a Gaussian radial distribution with characteristic radius of 5 nm. The SOI DG-FeTFET in TCAD simulation is biased to off-state ($V_{\rm g} = 0$ V) with the drain terminal at 0.5 V, while the substrate and source electrodes are grounded.

Results and discussion. Figure 1(c) shows the SET drain current for SOI DG-FeTFET with different LETs at $V_{\rm d} = 0.5$ V. The drain transient leakage current gradually increases to a max-

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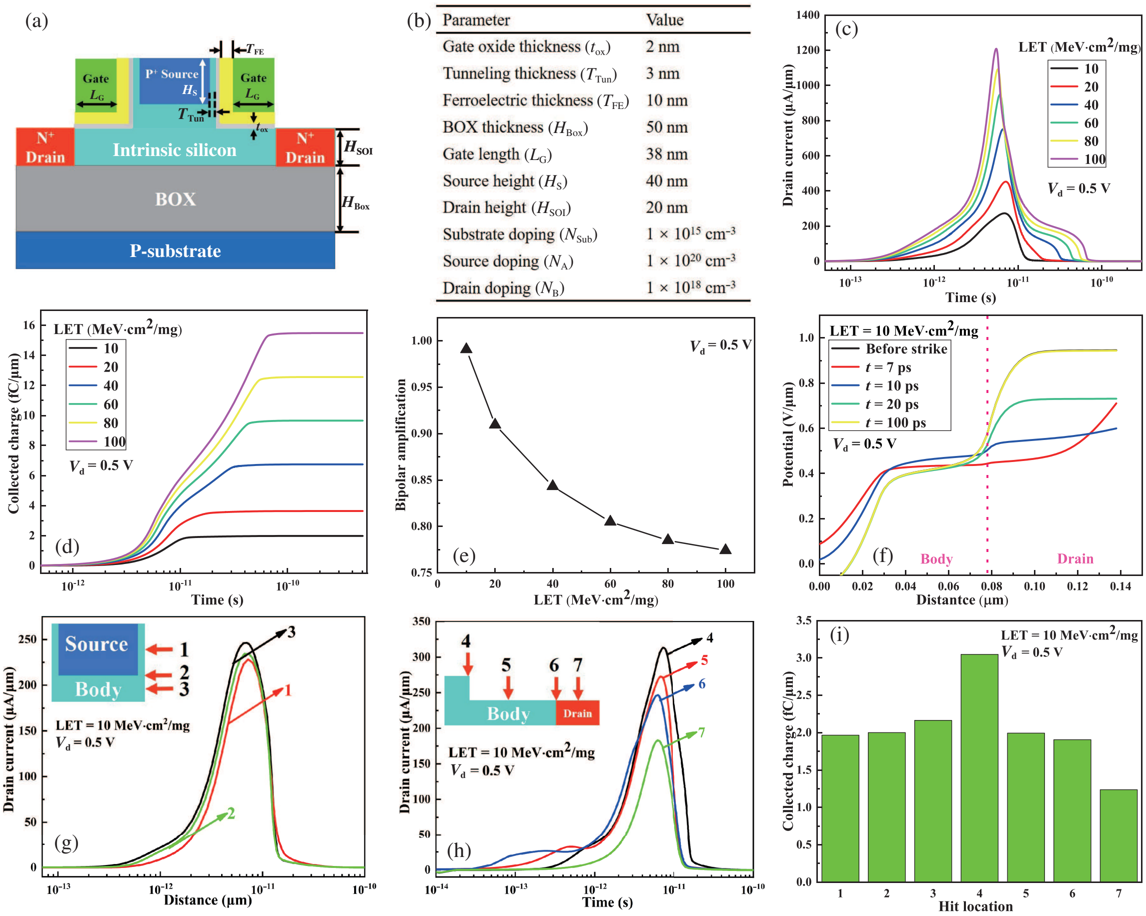

(b)

Parameter	Value
Gate oxide thickness (t_{ox})	2 nm
Tunneling thickness (T_{Tun})	3 nm
Ferroelectric thickness (T_{FE})	10 nm
BOX thickness (H_{Box})	50 nm
Gate length (L_G)	38 nm
Source height (H_S)	40 nm
Drain height (H_{SOI})	20 nm
Substrate doping (N_{Sub})	1×10^{15} cm^{-3}
Source doping (N_A)	1×10^{20} cm^{-3}
Drain doping (N_B)	1×10^{18} cm^{-3}

Figure 1 (Color online) Simulation results of SOI DG-FeTFET at $V_g = 0$ V and $V_d = 0.5$ V. (a) Cross-section schematic of DG-FeTFET; (b) physical parameters for TCAD simulation; (c) single event transient drain current with respect to various LETs; (d) time variations of collected charge with various LETs; (e) bipolar amplification as function of LETs; (f) horizontal distance variations of electrostatic potential with various time for DG-FeTFET at $V_d = 0.5$ V, at 2 nm below the lateral oxide/Si interface; (g) transient current induced by horizontal incidence; (h) transient current induced by vertical incidence; (i) collected charges for different strike positions.

imum value after ions bombard the sensitive region, which exhibits a typical single pulse mode. Under the mechanisms of carriers drift diffusion and electron-hole (e-h) pairs collection, because ionized e-h pairs increase with larger LET, the peak value of current collected by the drain terminal in DG-FeTFET increases from 2.72×10^{-4} A at 10 MeV·cm^2/mg to 1.20×10^{-3} A at 100 MeV·cm^2/mg, which is much larger than the on-state current ($I_{\rm on} = 7.63 \times 10^{-5}$ A). This may change the logical state of the electronic system and affect subsequent circuits stability. Figure 1(d) shows the variation of collected charge ($Q_{\rm coll}$) with respect to LET values for DG-FeTFET. The collected charge enters the saturation region after exponential increase. According to [8], for MOSFET, $Q_{\rm coll}$ increase slowly after exponential growth, which are different from TFET in this study. This disparity may suggest that the bipolar amplification effect is ubiquitous in MOSFET, but the bipolar amplification effect of DG-FeTFET is ignorable (the value of bipolar amplification effect is less than 1), as shown in Figure 1(e).

Figure 1(f) shows the change in 2-D electrostatic potential with time for DG-FeTFET, where is 2 nm below the lateral silicon film surface. The electrostatic potential increases gradually from the body to the drain before ion bombardment, the barrier between body and drain decreases after the ion has struck the channel, which allows the electrons generated by irradiation to be more easily collected by the drain electrode, which leads to a reduction in the transient duration when LET = 10 MeV·cm^2/mg.

The impact of several heavy ion striking locations between the source contact and the drain contact are analyzed in Figure 1(g) and (h) for DG-FeTFET. The peak of transient current increases when the strike position moves from the source (location 1) to the body (location 3), as shown in Figure 1(g). The maximum value of the drain current decreases when the hit location moves from the body (location 4) to the drain (location 6), as shown in Figure 1(h). The maximum collected charge corresponds to ion striking near the body region adjacent to the tunneling layer (location 4), while the minimum collected charge value corresponds to the hit position in the drain (location 7), as shown in Figure 1(i). When the strike position is closer to the body in the adjacent tunneling layer, the transient current peak is larger and more charges are collected. This is because the maximum electric field is located in the body below the source and near the corner of the tunneling layer. This indicates that the sensitive area for single event effect (SEE) in DG-FeFET is the body region next to the tunneling junction.

Conclusion. The mechanisms of SET in DG-FeTFET were investigated by TCAD simulation to assess the impact of the LET and the bombardment location of heavy ion on the transient responses. For LET larger than 10 MeV$\cdot$cm^2/mg, the maximum drain current is higher than the on-state current for DG-FeTFET. Thus, the DG-FeTFET is more susceptible to SET. Moreover, the bipolar amplification effect of DG-FeTFET is negligible. Additionally, the reduction of the body-drain barrier makes it easier for the holes to reach the drain and then recombine with the electrons to reduce the transient duration. According to our analysis, the region sensitive to bombardment is located in the channel near the transverse source/channel interface, where the electric field is larger. These results can provide some useful guidance for the design of DG-FeTFET-based anti-radiation logic circuits design.

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