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A 143.2–168.8-GHz signal source with 5.6 dBm peak output power in a 130-nm SiGe BiCMOS process

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Dear editor,

With the development of silicon-based processes, a variety of RF devices have become possible to be designed at frequencies above 100 GHz [1]. Besides, sub-terahertz systems operating in D-Band have the potential to be applied to a wide range of applications, such as high-resolution radar, energy detection, and broadband ultra high-speed communication [2]. However, for these applications, the generation of a D-Band signal source with milliwatt level output power, better phase noise, and wider tuning range remains a big challenge.

Various researches have been carried out for the implementation of the D-Band signal source. Among them, three methods are widely used, and they are the fundamental oscillator, the harmonic oscillator, and the multiplier with low-frequency signal source. The fundamental oscillator has been widely used, while the tuning range is limited owing to parasitic capacitance introduced by layout. The harmonic oscillator is relatively easy to implement wide tuning range, but the output power is limited. The more traditional approaches are still based on multiplier chain with low-frequency oscillator [1].

However, as we all know, the multiplier chains have many unwanted harmonic components. These harmonic signals would create multiple intermodulation components in the D-Band signal source and distort the phase noise. Therefore, it is necessary to suppress these unwanted harmonics for better phase noise [3].

In this study, we present a D-Band signal source that demonstrates 5.6 dBm peak output power at 159 GHz, as shown in Figure 1(a). By applying high pass matching networks in tripler and doubler design, the signal source achieves a comparable unwanted harmonics suppression of over 30 dBc in the whole output tuning range. Also, by analyzing the influence of the input power level (which was detected at the output of the E-Band tripler through power detector) and the base bias voltage on the output power of the D-Band doubler, implementation of the doubler has been carefully designed for higher output power.

24–28 GHz VCO and divide-by-4 design. This VCO is based on our previous study reported in [4]. Differential topology is adopted owing to the advantage of the virtual RF ground node for better phase noise and higher output power. Special attention is paid to symmetry during the VCO layout design to obtain better fundamental signal suppression, which in turn leads to better phase noise. Static topology frequency divider is adopted owing to the strict requirements of low input power level and high sensitivity. The divide-by-4 is achieved by cascading two stages of D-latch topology-based static divide-by-2 in an ac-coupled manner.

E-Band tripler design. The third harmonic en-

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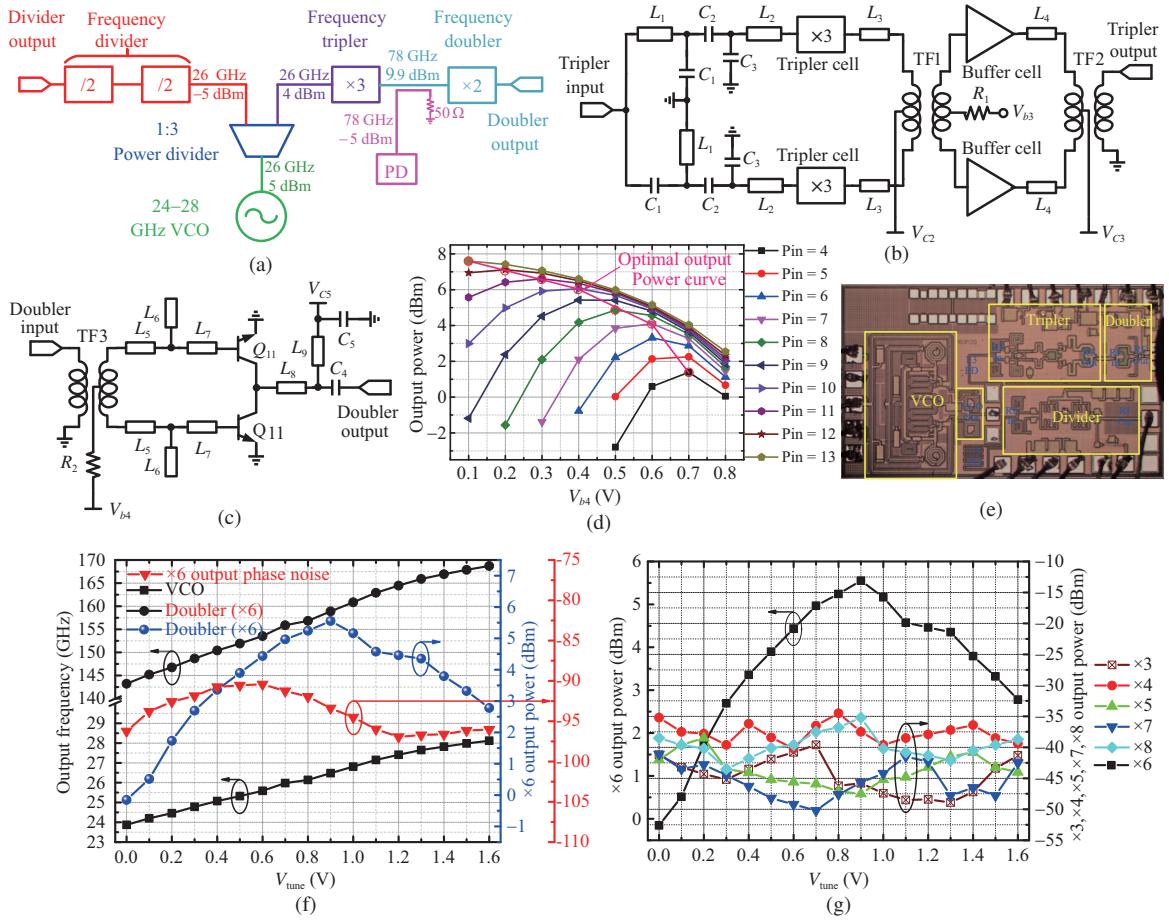

Figure 1 (Color online) (a) Block diagram of the D-Band signal source; (b) schematic of the E-Band tripler; (c) schematic of the D-Band doubler; (d) simulated output power of the D-Band doubler versus input power and base bias voltage at 78 GHz; (e) die micrograph of the signal source; (f) measured output frequency and phase noise vs. the tuning voltage $V_{\rm tune}$ of VCO; (g) measured output power and harmonic suppression vs. the tuning voltage $V_{\rm tune}$ of VCO.

hanced tripler is adopted owing to its wide tuning range and relatively low input power requirement [5], as depicted in Figure 1(b). Transformers (TFs) are used for the tripler impedance matching. In E-Band, the majority of the TF has characteristics that are single-turn coil and stacked coupling structure [6,7]. However, in the design of cascaded cascode topology differential circuits, the real part of the next stage input impedance is usually several times or a fraction of the previous stage output impedance. So it is difficult to well match the cascaded cascode topology with a single-turn TF according to the impedance transformation theory. One effective approach to well match these impedances with large difference is to use TF with metals turn ratio of 1:n ($n \geqslant 2$). However, this method will greatly increase the parasitic resistance and capacitance of the TF, thereby deteriorating the quality factor of the TF and affecting the operating bandwidth.

In our design, the methodology to co-design a single turn TF with a series inductance is presented. The output impedance of the tripler can be well transferred into a conductance circle with the adopted tuning inductance L_3 where the impedance matching can be implemented by a single turn TF easily [8]. The output of the tripler is designed along with a passive 15 dB coupler, allowing for accurate detection of its output power.

D-Band doubler design. The D-Band doubler is the most critical component in this D-Band signal source design because it directly determines the output power and the quality of the final output signal. Figure 1(c) shows the circuit schematic of the proposed D-Band doubler. As presented in [9], the base bias voltage of the doubler core will affect the output power. In the design process, we found that not only the base bias voltage but also the input power has a great influence on the output power. Figure 1(d) shows the output power of the doubler as a function of the input power and the base bias voltage V_{b4} at 78 GHz. It is obvious that the optimal output power of the doubler corresponds to different base bias point at different in-

put power level. Besides, as the input power level increases, the dc bias voltage V_{b4} that corresponds to the optimal output power gradually decreases. Therefore, the output power of the E-Band tripler must be carefully detected at different frequency, to obtain an optimum dc bias voltage for maximizing the output power of the D-Band doubler. Thus, an passive RF power detector is inserted between the E-Band tripler and the D-Band doubler to accurately detect the RF signal power level that entering the D-Band doubler. Then, the dc bias voltage of the D-Band doubler is determined based on the output dc voltage of the power detector for optimum output power at different frequencies.

Fabrication and measurement. Chip micrograph of the D-Band signal source is shown in Figure 1(e). The size of the chip including pads is 2 mm ×1.2 mm. The chip is tested through on wafer probing with dc pads bonded to printed circuit board to provide dc power. For output frequency test, the OML WR05 harmonic mixer with Keysight spectrum analyzer N9030A is used. The corresponding ×3, ×4 and ×5 harmonics are measured using N9030A with the OML WR08 harmonic mixer. The measured output frequency vs. the tuning voltage $V_{\rm tune}$ is illustrated in Figure 1(f). When the tuning voltage $V_{\rm tune}$ is tuned from 0 to 1.6 V, the measured output frequency of the VCO is from 23.8 to 28.1 GHz and corresponding output frequency of the signal source is from 143.2 to 168.8 GHz. Harmonic signal suppression is obtained by the difference between the harmonic signal (×3, ×4, ×5, ×7 and ×8) output power and the effective RF signal (×6) output power on the spectrum analyzer. Figure 1(g) plots the measured output power of the unwanted harmonics rejection. Benefit from the proposed unwanted harmonics suppression technique in the tripler and doubler design, the unwanted harmful harmonics rejection are better than 30 dBc over the entire tuning range.

For output power test, the VDI Erickson PM4 power meter with the WR05-to-WR10 waveguide transition are adopted to detect the output power. The measured output power vs. the tuning range is plotted in Figure 1(g). The signal source achieves a measured peak output power of 5.6 dBm at 159 GHz, and the output power is higher than 0 dBm when the tuning voltage $V_{\rm tune}$ changes from 0.1 to 1.6 V. The phase noise of the signal source is measured at the divide-by-4 output by RS FSUP50 spectral analyzer, because it is difficult and inaccurate to measure the phase noise directly at the D-Band doubler output port. The measured phase noise of the signal source is shown in Figure 1(f). As illustrated in Figure 1(f), the measured phase noise is around −93 dBc/Hz @ 1 MHz between 142–168 GHz frequency range.

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Supporting information Appendixes A–E. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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