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• **SUPPLEMENTARY FILE** •

A 143.2-168.8-GHz Signal Source with 5.6 dBm Peak Output Power in a 130 nm SiGe BiCMOS Process

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Abstract A 143.2-168.8 GHz signal source with 5.6 dBm peak output power at 159 GHz and corresponding -94 dBc/Hz @ 1 MHz phase noise is reported. The circuit includes a 26 GHz Colpitts topology voltage-controlled-oscillator and a static divide-by-four chains, an E-Band frequency tripler, a balanced D-Band frequency doubler. Through systematically analyzing the influence of input power level (detected by power detector) and base bias voltage on the output power of active frequency doubler, implementation of the D-Band doubler has been carefully designed to maximize output power of the signal source. Besides, by adopting high pass matching network in frequency tripler and frequency doubler design, the signal source exhibits an excellent unwanted harmonics suppression of over 30 dBc in the whole output tuning range. The total chip area is 2.4 mm^2 and the whole DC power consumption is 379 mW, which resulting in a peak DC-to-RF efficiency of 1.14 %. Compared with other D-Band signal sources, this signal source achieves the best phase noise (with divider chain), very competitive tuning bandwidth and the highest output power while using silicon-based processes with the lowest cutoff f_T frequency.

Keywords

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1 Appendix A

The circuit system block diagram of the active D-Band signal source is illustrated in Fig. 1 and consists of a 24-28 GHz voltage controlled oscillator (VCO), a one to three transmission line based passive power divider, two cascaded D-latch based static frequency dividers, an E-Band active frequency tripler, an E-Band power detector, an E-Band 15 dB passive coupler and a D-Band active frequency doubler. The circuit is designed using Global Foundries (GF) 130 nm SiGe BiCMOS technology. According to [15], $f_{MAX}/3$ is the characteristic frequency point up to which radio frequency (RF) amplifier can get relatively good performance, mainly refers to signal gain and output power. f_{MAX} of this process is 250 GHz, so D-Band active frequency doubler instead of D-Band amplifier was designed as the final stage of the signal source to provide maximum output power. Besides, center frequency of the oscillator is set to be around 26 GHz, mainly because it is the frequency up to which good phase noise, moderate output power (higher than 5 dBm) and wide tuning bandwidth can be achieved in the chosen process based on our previous design. The input of the E-Band power detector is connected to the coupling end of the E-Band 15 dB coupler, which is inserted between the E-Band tripler and D-Band doubler, to accurately detect the

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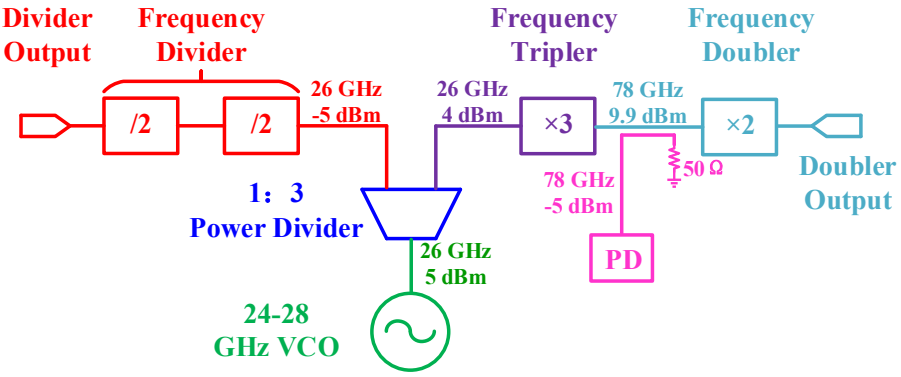

Figure 1 Circuit block diagram of the active D-Band signal source.

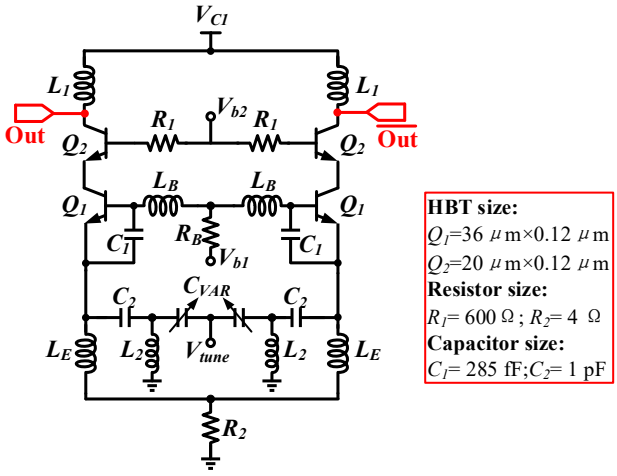

Figure 2 Schematic of the differential Colpitts oscillator.

output power of the E-Band tripler. The input power level of the tripler needs to be higher than 2 dBm between 24-28 GHz. Cascaded static frequency divider chains were adopted to divide the VCO output to about 6.5 GHz for the convenience of employing an off-chip phase locked loop based on our previous work [16], and also facilitate phase noise measurement of this signal source at the same time. The normal operation of the frequency divider chains require an input power higher than -8 dBm. Besides, the signal source is designed to deliver more than 5 dBm output power at around 150 GHz, so the input power of the D-Band doubler needs to be higher than 5 dBm. Considering the interconnection loss between the 24-28 GHz VCO and the E-Band tripler, the E-Band tripler and D-Band doubler, we have reserved some margin for the power budget of each device as illustrated in Fig. 1. All devices are designed with differential structure for better common-mode signal rejection. In addition, matching networks of the active frequency tripler and doubler all exhibit high pass characteristic to further suppress the unwanted harmful harmonics.

2 Appendix B

Circuit schematic of the differential topology Colpitts VCO is depicted in Fig. 2, which is based on our previous work reported in [17]. Differential topology is adopted due to the advantage of virtual RF ground node for better phase noise and higher output power meanwhile. Besides, cascode configuration is adopted in the VCO core rather than common emitter topology based buffer to achieve better resonant

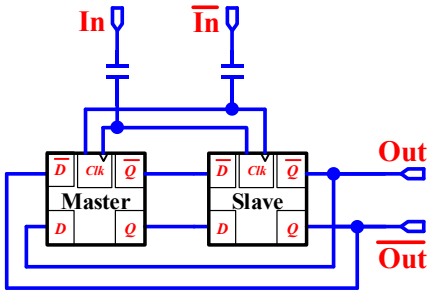

Figure 3 Block diagram of the differential static frequency divider.

tank isolation and RF power gain, which is caused by higher gain of common base topology buffer stage compared with common emitter topology buffer at this frequency range [18]. In addition, the VCO design process pays special attention to symmetry design of the layout to obtain better fundamental signal suppression, which in turn leads to better phase noise.

The Colpitts VCO consists of a differential structure transistor pair Q_1 and Q_2 and a resonant cavity, which is composed of symmetrically distributed base inductor L_B and an equivalent capacitance consisting of C_1 and C_{VAR}. The ac-coupling approach was adopted for the oscillation signal in the resonant tank, which is realized by using inductance L_2 and capacitance C_2 for the varactors biasing. Then we can take advantage of the whole positive tuning characteristic of the varactors [19]. Resistor R_2 is adopted as current biasing element rather than a traditional current mirror to prevent considerable 1/f noise coming from additional introduced active devices. The inductances (L_1, L_2, L_B, L_E) adopted in the VCO are composed of the thickest top metal layer AM of this process for better insertion loss, while the ground is shielded by the intermediate layer metal MQ to form a grid-like structure for higher quality factor of the inductor. Besides, the ground plane of the VCO is composed of the intermediate layer metal MQ, such that all the RF signal lines are composed of top two thick layers of metal AM and LY located above the ground plan, and all of the dc feeders are composed of bottom two thin layers of metal M1 and M2 located below the ground plane. By distributing the RF lines and dc feeders on both sides of the ground plane, it is also possible to effectively reduce coupling between them and improve the performance of the oscillator.

3 Appendix C

In the D-Band signal source design, the output signal power of VCO is preferred to be transferred to the multiplier chains as much as possible to maximize the output power, with only a small amount of power is used to drive the frequency divider chains. Millimeter wave frequency dividers are usually implemented by dynamic topology, because dynamic frequency divider is easier to operate at higher frequency without latching mechanism [2]. However, the input sensitivity of dynamic frequency divider is relatively poor, which is unacceptable in our design. In contrast, static frequency divider shows better input sensitivity owing to its self-oscillation. Based on the strict requirements of low input power level and high sensitivity, static topology frequency divider was adopted in our design.

The circuit system block diagram of the static frequency divider is shown in Fig. 3. The input differential clock signal is converted by an on-chip LC balun for better chip size in this frequency range. The internal dividing function is realized by connecting the differential inverted slave stage output to the differential master stage input [20]. Schematic of the D-latch that comprises the core of this static frequency divider is shown in Fig. 4. The DC bias point of Q positive and Q negative are set to be the same value as the input DC bias point of D positive and D negative, so that the master and slave can be directly connected with each other and avoid using of additional bias circuits. In addition, ac-coupling (through a 1 pF capacitor) was adopted to cascade the two frequency dividers and special care is given to divider layout design, mainly the symmetry and compactness of latch layout. The final divide-by-four is

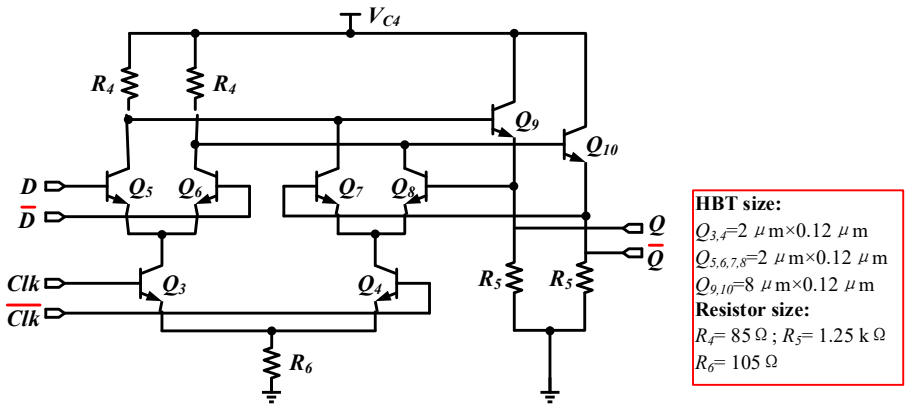

Figure 4 Schematic of D-latch of the static frequency divider.

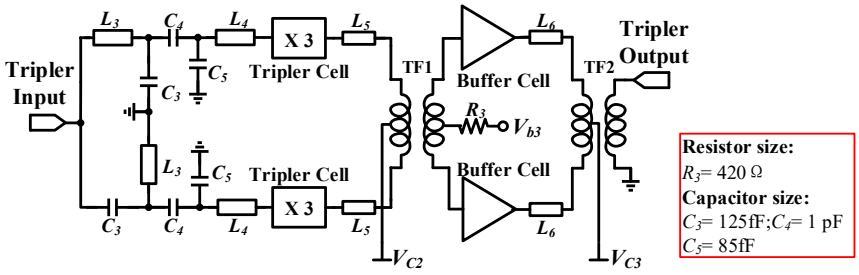

Figure 5 Schematic of the E-Band differential frequency tripler.

achieved by cascading two stages of D-latch topology based static divide-by-two in an ac-coupled manner. Besides, one of the differential output port of the divide-by-four is directly connected to a 50 Ω resistor for the convenience of test, while the other one is delivered to an output RF ground signal ground (GSG) PAD to facilitate phase noise measurement of the signal source.

4 Appendix D

Due to high loss of passive components in millimeter-wave band and effect of parasitic parameters, this D-Band signal source was realized by cascading a 24-28 GHz VCO with frequency tripler and doubler. There are several techniques currently used for frequency tripler design, including third harmonic output power enhanced tripler, double diode based tripler and injection locked frequency tripler. The third harmonic enhanced tripler was adopted in our design for the concern of its wide tuning range and its relatively low input power requirement [21]. Circuit schematic of the E-Band frequency tripler is depicted in Fig. 5 and comprises a cascode structure differential tripler core and a cascode structure differential buffer stage. The input of the tripler before tripler cell is composed of a typical LC balun that composed of microstrip line L_3 and MIM capacitor C_3 for generating a differential signal, and one stage matching network that composed of series transmission line L_4 and parallel capacitors C_5. The MIM capacitor C_4 is a 1 pF capacitor for DC blocking. Differential topology was adopted in our design since it offers higher output power, higher common mode rejection and better even harmonic suppression.

Table 1 Comparison of state of art frequency triplers

Frequency [GHz]	70	75	80	85
Z_{out_diff} of Tripler	6.4+j*215.5	6.9+j*198	7.2+j*183	7.5+j*169
Z_{in_diff} of Buffer	29.6-j*20.7	29.5-j*19.4	29.4-j*18.2	29.3-j*17.2

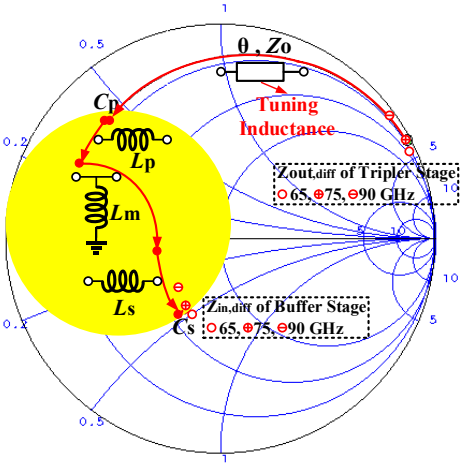

Figure 6 Matching procedure of TF1 of the E-Band tripler on the Smith Chart.

Because of the broadband impedance matching characteristic and moderate chaip area of the transformer, transformers (TF) were used for the E-Band frequency tripler core (TF1) and buffer output (TF2)impedance matching. In E-Band, the majority of the transformer have characteristics that single-turn coil and stacked coupling structure [22]. However, in the design of cascaded cascode topology differential circuits, real part of the next stage input impedance is usually several times or a fraction of the previous stage output impedance. So it is difficult to well match the cascaded cascode topology with a single-turn TF according to impedance transformation theory. One effective approach to well match these networks with large difference between input and output impedance is to use TFs with metal turns ratio of 1:n (n $\geqslant$ 2). However, this method will greatly increase the parasitic resistance and capacitance of the transformer, thereby deteriorating the quality factor of the transformer and affecting the operating bandwidth of the circuit. Besides, for lack of precise model of multi-turn metal TFs, EM simulation (which is very time consuming) was relied on only to accurately determine the size of multi-turns TFs.

In our design, the methodology to co-design a single turn TF with a series inductance is presented to well match an output single or differential impedance with large difference input impedance. Table 1 summarizes the output impedance of the differential tripler cell and the input impedance of differential buffer cell. Fig. 6 shows the circuit schematic of TF1 and the impedance matching process on Smith chart with the proposed method. It can be seen that the output impedance of the tripler can be well transferred into the conductance circle with the adopted tuning inductance L_5 where the impedance matching can be implemented by a single turn transformer easily [23]. Inductances L_p and L_s representing the self-inductance value of the primary and secondary windings of the transformer, while L_m represent the magnetizing inductance between the two windings [24]. Output impedance matching of the buffer cell was implemented in a similar way with the tuning inductance L_6. The output of the tripler is designed along with the 15 dB coupler that follows, allowing for accurate detection of its output power. Besides, the high pass characteristics of TF1 and TF2 can provide additional harmonic rejection ($\times$1,$\times$2) of the tripler.

The proposed E-Band tripler demonstrates a meadured 3 dB bandwidth ranging from 69 to 86 GHz. Besides, the tripler exhibits a peak output power of 9.9 dBm at 78 GHz with the input power level of 2 dBm. Peak conversion gain of the tripler is higher than 8 dB with 0 dBm input power at 26 GHz input frequency. The output power is higher than 7 dBm in the frequency range in which the signal source operates, which is sufficient to drive the D-Band doubler [21].

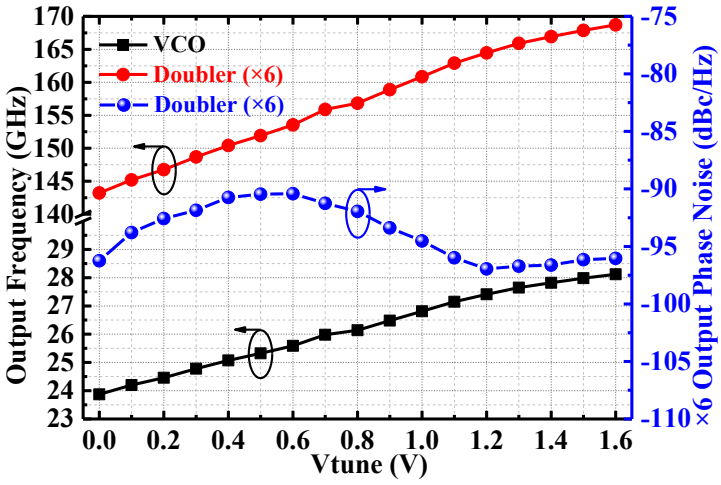

Figure 7 Measured output D-Band signal frequency and phase noise versus the tuning voltage V_{tune} of VCO.

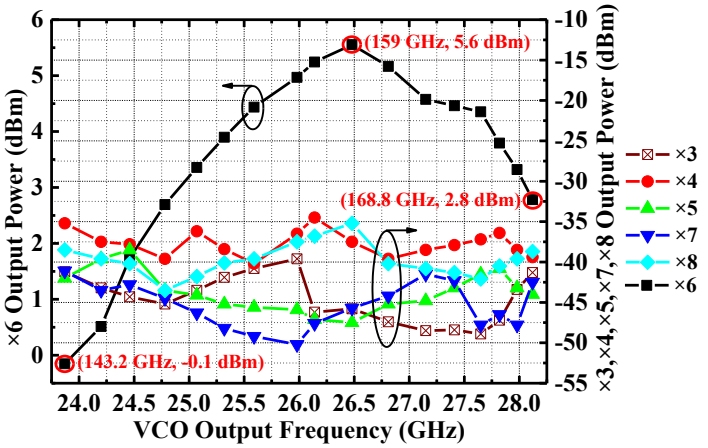

Figure 8 Measured output D-Band signal power and harmonic suppression versus the tuning voltage V_{tune} of VCO.

5 Appendix E

The voltage controlled oscillator, static frequency divider, E-Band frequency tripler and D-Band frequency doubler draw 44, 22, 48 and 21 mA from supplies of 2.8, 2.8. 3.3 and 1.7 V, respectively. Chip measurement of the signal source is divided into three parts: output signal frequency and harmonic rejection test, signal output power test, and signal phase noise test. Two on-wafer test setups were used to measure the output RF signal frequency (including harmonic rejection) and power. The looses caused by RF probe, waveguide transition and output Z-type waveguide have been carefully calibrated. The loss of the RF probe and waveguide transition is directly determined by the values given in the product manual, while the loss of the Z-type waveguide is obtained by testing its S_{21} with Keysight vector network analyzer and D-Band frequency extension.

For different tuning voltage, based bias voltage of the D-Band frequency doubler is set according to the DC level value of the power detector output for maximum output power. For example, the measured output frequency at the E-Band tripler output is about 75 GHz when the tuning voltage of VCO is 0.4 V, while the output power of the E-Band frequency tripler measured from the power detector is 9 dBm, so base bias voltage of the D-Band frequency doubler is set to be 0.4 V for maximum output power. The

Table 2 Comparison with state-of-the-art D-Band silicon-based signal source

Reference	[1]	[6]	[11]	[12]	[13]	**This work**
Circuit	Fundamental VCO	Harmonic VCO	VCO+×2	VCO+×3	VCO+×2	**VCO+×3+×2**
Frequency [GHz]	150.8-158.3	146	122.9-142.9	129-159	120-163	**143.2-168.8**
Peak P_{out} [dBm]	-3.5	9.5	-2	-8	3	**5.6**
Phase Noise [dBc/Hz]	-85@2MHz	-94@1MHz	-96.5@1MHz	-90@1MHz	-93@1MHz	**-96@1MHz**
DC Power [mW]	58	43.5	51	95	410	**379**
Tuning Range [%]	4.84	-	14.8	20.8	30.4	**16.5**
DC-to-RF Efficiency [%]	0.77	20.46	1.24	0.17	0.48	**1.14**
Area [mm^2]	0.71	0.39	0.23	0.075	1.05	**2.4**
FOM_1 [dBc/Hz]	-158.8	-	-178.3	-179.7	-179.5	**-178.6**
FOM_2 [dBc/Hz]	-155.3	-	-176.3	-171.7	-182.5	**-184.2**
f_T/f_{MAX} [GHz]	300/500	350/350	-/550	-/230	170/250	**200/250**
Technology	130nm SiGe	800nm InP	40nm CMOS	65nm CMOS	350nm SiGe	**130nm SiGe**

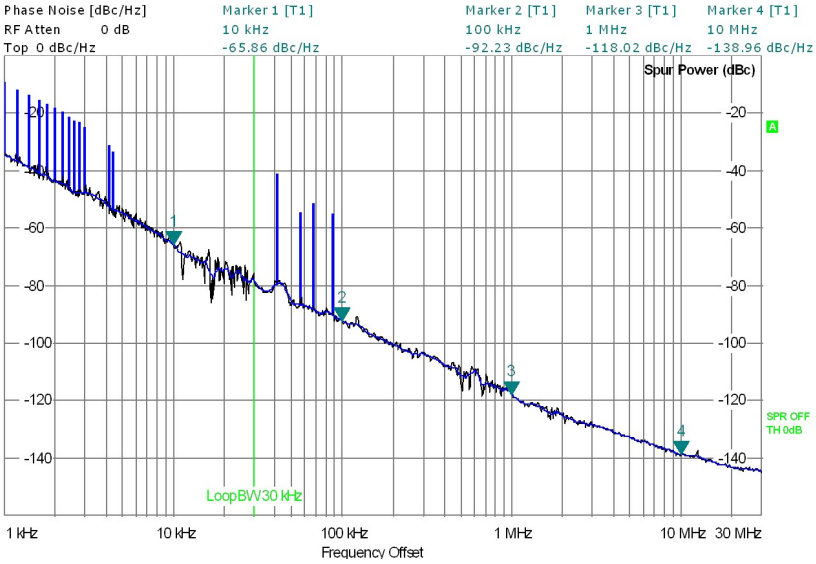

Figure 9 Measured phase noise of the signal source at divider output with VCO tuning voltage of 0.7 V (VCO output frequency is 25.98 GHz).

output power test process of other tuning voltage is similar. The final measured de-embedded output power versus the output frequency tuning range is plotted in Fig. 8. The D-Band signal source achieves a peak measured output power of 5.6 dBm at 159 GHz and the output power is higher than 0 dBm when the tuning voltage of VCO V_{tune} changes from 0.1 to 1.6 V.

The phase noise of the signal source is measured at the divide-by-four output by RS FSUP50 spectral analyzer, because it is difficult and inaccurate to measure the phase noise directly at the D-Band doubler output of the signal source. The measured phase noise at divider by four output is -118 dBc/Hz @ 1MHz at 6.5 GHz range, as shown in Fig. 9. The measured result corresponds to -90.4 dBc/Hz at 156 GHz frequency range (According to the relationship between phase noise and frequency multiple, a factor of 27.6 dB (20 log (24)) was added). The phase noise that contributed by divider chain and subsequent tripler and doubler is neglected [2,17]. The measured phase noise of the entire signal source versus the tuning voltage V_{tune} of VCO are shown in Fig. 7. As illustrated in Fig. 7, the measured phase noise of the signal source is around -93 dBc/Hz @ 1 MHz between 142 and 168 GHz frequency range.The figures of merits as illustrate in [17], FOM_1 (1) and FOM_2 (2) are included in Table 2. In FOM_2, the output RF power of the signal source is also included for comparison. It can be seen from Table 2 that the

designed D-Band signal source achieves the best FOM2 and very competitive FOM1 when comparing with other D-Band silicon based signal source.

$$FOM_1 = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) - 20\log\left(\frac{TR}{10}\right) \quad (1)$$

$$FOM_2 = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{diss}}{P_{out}}\right) - 20\log\left(\frac{TR}{10}\right) \quad (2)$$

References

1 U. Ali, M. Bober and A. Thiede.: 'Design of Voltage Controlled Oscillators (VCOs) in D-Band and their Phase Noise Measurements using Frequency Down-Conversion'. in Proc. Eur. Microwave Integrated Circuits Conf. (EuMIC), 2016, pp. 317-320

2 S. Shopov, A. Balteanu, J. Hasch, P. Chevalier, A. Cathelin and S. P. Voinigescu.: 'A 234-261-GHz 55-nm SiGe BiCMOS Signal Source with 5.4-7.2 dBm Output Power, 1.3 % DC-to-RF Efficiency, and 1-GHz Divided-Down Output', IEEE J. Solid-State Circuits, 2016, **61**, (9), pp 2054-2065

3 R. B. Yishay and D. Elad.: 'A 17.5 dBm D-Band Power Amplifier and Doubler Chain in SiGe BiCMOS Technology'. in Proc. Eur. Microwave Integrated Circuits Conf. (EuMIC), 2014, pp. 53-56

4 F. Ahmad, M. Furqan, B. Heinemann and A. Stelzer.: 'A SiGe D-Band Fundamnetal-Wave VCO with 9 dBm Output Power and -185 dBc/Hz FOMT'. in Proc. IEEE Compound Semiconductor Integr. Circuits Symp. (CSICS), 2015, pp. 1-4

5 P. Zhou, J.Chen, P. Yan. D. Hou and W. Hong.: 'High output power 243 GHz voltage controlled oscillator in a 130 nm SiGe BiCMOS process', Electronic Letters, 2018, **54**, (6), pp 348-350

6 M. Hossain, N. Weimann, W. Heinrich and V. Krozer.: 'Highly Efficient D-Band Fundamental Frequency Source on InP-DHBT Technology'. in Proc. Eur. Microwave Conf. (EuMC), 2018, pp. 1005-1008

7 U. Ali, G. Fischer and A. Thiede.: 'Low Power Fundamental VCO Design in D-Band Using 0.13 um SiGe BiCMOS Technology'. in Proc. German Microwave Conf. (GeMIC), 2015, pp. 359-362

8 S. Zeinolabedinzadeh, P. Song, M. Kaynak, M. Kamarei, B. Tillack and J. D. Cressler.: 'Low Phase Noise and High Output Power 367 GHz and 154 GHz Signal Sources in 130 nm SiGe HBT Technology'. in IEEE MTT-S International Microwave Symposium. (IMS), 2014, pp. 1-4

9 S. Muralidharan, K. Wu and M. Hella.: 'A 110-132 GHz VCO with 1.5 dBm Peak Output Power and 18.2 % Tuning Range in 130 nm SiGe BiCMOS for D-Band Transmitters'. in IEEE Silicon Monolithic Integrated Circuits in RF Sysyems. (SiRF), 2016, pp. 64-66

10 B. Khamaisi and E. Socher.: 'A 159-169 GHz Frequency Source with 1.26 mW Peak Output Power in 65 nm CMOS'. in Proc. Eur. Microwave Integrated Circuits Conf. (EuMIC), 2014, pp. 536-539

11 Y. Chang and H. Lu.: 'A D-Band Wide Tuning Range VCO Using Switching Transformer'. in IEEE MTT-S International Microwave Symposium. (IMS), 2017, pp. 1356-1359

12 H. Holisaz and S. S. Naeini.: 'A Low Noise D-Band VCO With a Wide Bandwidth and a Steady Output Power', IEEE Microw. Wireless Compon. Lett., 2015, **25**, (11), pp 742-744

13 C. Bredendiek, N. Pohl, K. Aufinger and A. Bilgic.: 'An Ultra-Wideband D-Band Signal Source Chip Using a Fundamental VCO with Frequency Doubler in a SiGe Bipolar Technology'. in IEEE Radio Frequency Integrated Circuits (RFIC), 2012, pp. 83-86

14 D. Hou, J. Chen, P. Yan and W. Hong.: 'A 270 GHz ×9 Multiplier Chian MMIC With On-Chip Dielectric-Resonator Antenna', IEEE Trans. Terathz. Scienc and Tech., 2018, **8**, (2), pp 224-230

15 N. Sarmah, P. Chevalier and U. R. Pfeiffer.: '160-GHz Power Amplifier Design in Advanced SiGe HBT Technologies With Psat in Excess of 10 dBm', IEEE Trans. Microw. Theory Tech., 2013, **61**, (2), pp 939-947

16 Z. Chen, M. Wang, J. Chen, W. Liang, P. Yan, J. Zhai, W. Hong.: 'Linear CMOS LC-VCO Based on Triple-Coupled Inductors and Its Application to 40-GHz Phase-Locked Loop', IEEE Trans. Microw. Theory Tech., 2017, **65**, (8), pp 2977-2989

17 Z. Peng, D. Hou, J. Chen, Y. Xiang and W. Hong.: 'A 28 GHz Low Phase-Noise Colpitts VCO with Wide Tuning-Range in SiGe Technology'. in IEEE Radio Frequency Integration Technology (RFIT), 2018, pp. 1-3

18 H. Li and H-M. Rein.: 'Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe bipolar production technology', IEEE J. Solid-State Circuits, 2003, **38**, (2), pp 184-191

19 G. Sapone, E. Ragonese, A. Italia and G. Palmisano.: 'A 0.13 um SiGe BiCMOS Colpitts-Based VCO for W-Band Radar Transmitters', IEEE Trans. Microw. Theory Tech., 2013, **61**, (1), pp 185-194

20 Y. Sun, et al.: 'A Low-Phase-Noise 61 GHz push-push VCO with Divider Chain and Buffer in SiGe BiCMOS for 122 GHz ISM Application'. in IEEE Radio Frequency Integrated Circuits (RFIC), 2012, pp. 79-82

21 P. Zhou, J.Chen, H. Li, D. Hou, P. Yan, C. Yu and W. Hong.: 'A High-Efficiency E-Band SiGe HBT Frequency Tripler With Broadband Performance'. in IEEE MTT-S International Microwave Symposium. (IMS), 2018, pp. 690-693

22 C. Chou, Y. Hsiao, Y. Wu Y. Lin, C. Wu and H. Wang.: 'Design of a V-Band 20-dBm Wideband Power Amplifier Using Transformer-Based Radial Power Combining in 90-nm CMOS', IEEE Trans. Microw. Theory Tech., 2016, **64**, (12), pp 4545-4560

23 A. Sarkar, F. Aryanfar and B. A. Floyd.: 'A 28-GHz SiGe BiCMOS PA With 32% Efficiency and 23-dBm Output Power', IEEE J. Solid-State Circuits, 2017, **52**, (6), pp 1680-1686
24 J. R. Long.: 'Monolithic Transformers for Silicon RF IC Design', IEEE J. Solid-State Circuits, 2000, **35**, (9), pp 1368-1382
25 L. Wang, Y. Xiong, B. Zhang, S. Hu and T. Lim.: 'Millimeter-Wave Frequency Doubler With Transistor Grounded-Shielding Structure in 0.13 um SiGe BiCMOS Technology', IEEE Trans. Microw. Theory Tech., 2011, **59**, (5), pp 1304-1310
26 K. Wu, S. Muralidharan and M. M. Hella.: 'A Wideband SiGe BiCMOS Frequency Doubler With 6.5-dBm Peak Output Power for Millimeter-Wave Signal Sources', IEEE Trans. Microw. Theory Tech., 2018, **66**, (1), pp 187-199
27 T. Fujibayashi, Y. Takeda, Y. S. Teh, W. Stapelbroek, S. Takeuchi and B. A. Floyd.: 'A 76- to 81- Multi-Channel Radar Transceiver', IEEE J. Solid-State Circuits, 2017, **52**, (9), pp 2226-2241