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Effective gate length model for asymmetrical gate-all-around silicon nanowire transistors

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Dear editor,

With the development of VLSI technology, gate-all-around (GAA) silicon nanowire transistor (SNWT) has emerged as one of the most potential candidates for ultimately scaled CMOS devices at the end of the technology roadmap. Some pioneering research studies have demonstrated super scalability and high performance with GAA SNWT [1–3]. Whereas, in the practical fabrication results [1,2], the all-around gate electrode was usually not ideally symmetrical about the central axis of nanowire, but in a trapezoidal cross section along the nanowire axial direction owing to the shadowing effect of nanowire to the etching process. Such asymmetry of gate electrode will make the performance evaluation incorrect and result in inaccuracy in device compact model for circuit simulation. However, there still lack of research on modeling of asymmetrical GAA silicon nanowire MOSFETs [4, 5]. In this study, we establish an effective gate length model of GAA SNWT with asymmetrical gate and verify it with technology-computer-aid-design (TCAD) simulation. With the proposed model, the asymmetrical GAA SNWT can be treated as an equivalent symmetrical device so that the modeling parameters can be simplified in circuit simulation.

Simulation and methodology. The cross-sections of GAA SNWTs with asymmetrical gates are depicted in Figure 1(a) along channel direction. In this device, the nanowires are silicon cylinders with radius of r and wrapped by gate oxide with thickness of t_{ox}. The source and drain are connected to nanowires and extended to be a cubic for reducing the parasitic resistance. The gate length l is then defined as the intersection of gate electrode with the gate oxide surface. In the practical GAA SNWT fabrication process, l usually varies along the gate oxide surface just as shown in Figure 1(a). Owing to the non-ideal dry etching of gate electrode and the shadowing effect of nanowire to the bottom gate formation, the cross-section of gate electrode along the nanowire axial direction is usually a trapezoid shape with the top side length of l_1 and the bottom side length of l_2. Normally, l_1 is determined by the layout and lithography process, i.e., the apparent gate length.

In this study, all the current-voltage characteristics of GAA SNWTs are obtained by three-dimensional TCAD simulation tool, the Synopsys licensed device simulator Sentaurus. To accurately simulate the ultra-scaled GAA SNWTs, quantum potential model, surface scattering related mobility model and non-equilibrium carrier transportation equations are taken into account in the simulation. All the models have been calibrated in the previous studies [6, 7]. The simulated GAA SNWTs in this paper are n-type MOSFET with r of 3 nm and t_{ox} of 0.9 nm.

Figure 1(b) compares the simulated I_D-V_G char-

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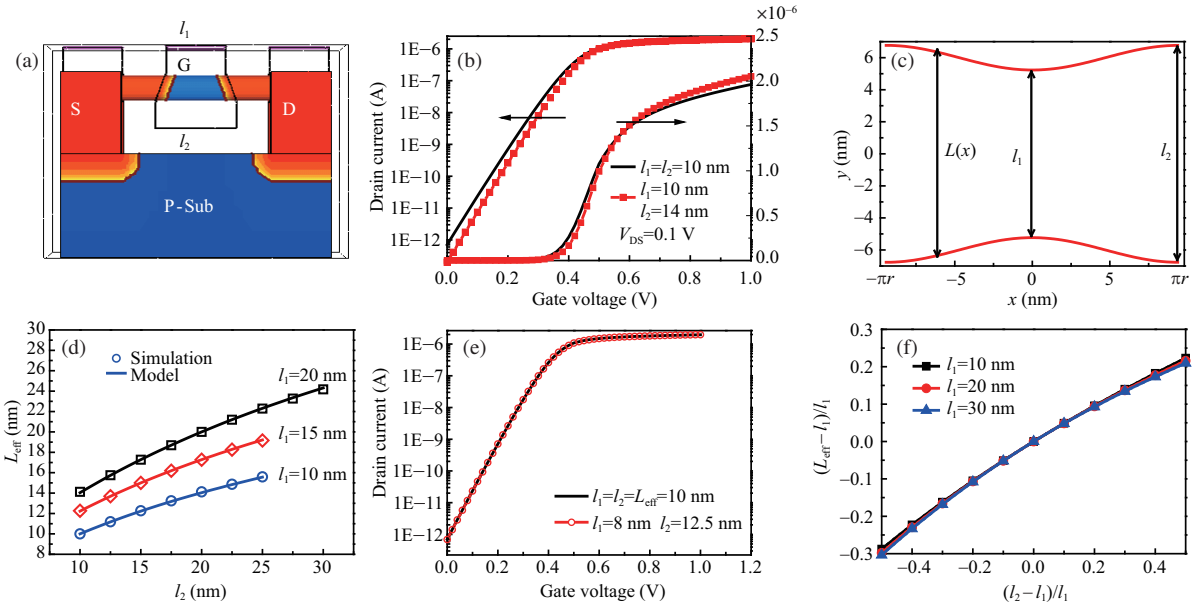

Figure 1 (Color online) (a) The cross section view of GAA SNWTs with non ideal structure ($l_1 \neq l_2$); (b) comparison of the I_D-V_G characteristics of GAA SNWTs with symmetrical and asymmetrical gate structure; (c) the unfolded drawing of the asymmetrical gate cut l_2 to form two cosine shaped gate edges; (d) the effective gate length changes with l_2 when l_1 is constant; (e) comparison of I_D-V_G characteristics between the asymmetrical GAA SNWT and the equivalently symmetrical device; (f) the relative change of L_{eff} to l_1 compared to the change of l_2.

acteristics of GAA SNWTs with symmetrical and asymmetrical gate lengths. On the I_D-V_G curves, the threshold voltage V_T is defined as the gate voltage at which the drain current equals to 100 nA × W_{eff}/l_1, where W_{eff} is the perimeter of nanowire and l_1 the apparent gate length. As shown in Figure 1(b), V_T of the symmetrical GAA SNWT with $l_1 = l_2 = 10$ nm is extracted to be 0.38 V and that of the asymmetrical GAA SNWT with $l_1 = 10$ nm and $l_2 = 14$ nm becomes 0.40 V. The higher V_T of the asymmetrical GAA SNWTs is mainly owing to better short channel effect control by longer bottom gate length l_2 even though the apparent gate length l_1 is same as the symmetrical device. On the other hand, the drain current of asymmetrical GAA SNWT also becomes higher than that of symmetrical device owing to lower source/drain series resistance electrically induced by longer bottom gate. It indicates that the asymmetry of all-around gate electrode indeed affects the electrical characteristics of GAA SNWTs. An accurate model for effective gate length L_{eff} is then necessary to simulate the asymmetrical GAA SNWTs.

To calculate the effective gate length L_{eff}, a symmetrical GAA SNWT is defined as the equivalent device to an asymmetrical one as their linear drain current I_D are same each other. Then L_{eff} is defined as the apparent gate length l_1 of the equivalent symmetrical device.

According to [8], the threshold voltage V_T of short channel MOSFETs can be obtained. With V_T model, the linear I_D of any MOSFET with uniform gate length L and gate width W can be calculated as

$$I_D = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right). \quad (1)$$

When applying this equations to calculate linear I_D of an asymmetrical GAA SNWT, it has to be divided into infinitely many microelement transistors along the gate width direction with an infinitely small width dw. Then the linear I'_D of an asymmetrical GAA SNWT can be calculated as the integral of the current of all microelement transistors, expressed as

$$I'_D = \int \frac{\mu C_{ox}}{L(w)} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right) \mathrm{d}w, \quad (2)$$

where $L(w)$ is the gate length along gate width direction.

To obtain $L(w)$, the three-dimensional gate electrode has to be unfolded into a planar structure. It can be proven that the intersection of an asymmetrical gate with gate oxide surface is an ellipse if assuming that the gate electrode has the trapezoid cross section along channel direction. The gate edges then can be cut along the bottom gate length l_2 and unfolded into two cosine shaped curves as shown in Figure 1(c). The $L(w)$ can then be ex-

pressed as

$$L(w) = \frac{1}{2}\left(l_1 + l_2 + \frac{r}{r + t_{\rm ox}}(l_1 - l_2)\cos\left(\frac{w}{r}\right)\right). \tag{3}$$

By calculation and comparison, the effective gate length $L_{\rm eff}$ can be expressed as

$$L_{\rm eff} = -2\lambda \ln\left(\frac{\sqrt{8S+1}-1}{4}\right), \tag{4}$$

where S is the function of l_1, l_2, r, $t_{\rm ox}$ and the natural length λ. For GAA SNWTs, λ can be calculated as below according to [9]:

$$\lambda = \sqrt{\frac{2\varepsilon_{\rm Si} r^2 \ln(1 + \frac{t_{\rm ox}}{r}) + \varepsilon_{\rm ox} r^2}{4\varepsilon_{\rm ox}}}. \tag{5}$$

Results and discussion. To verify the effective gate length model of asymmetrical GAA SNWTs, Eq. (4) is compared to the simulated results in Figure 1(d). To obtain the effective gate lengths of different asymmetrical GAA SNWTs from the TCAD simulation results, their threshold voltages are compared to those of symmetrical GAA SNWTs with different apparent gate lengths and the effective gate length is calculated by interpolation. From the comparison in Figure 1(d), it could be seen that the compact model shows high accuracy in matching to the TCAD simulation results at different l_1 and l_2.

To identify the effectiveness of threshold voltage criteria in defining equivalent devices, an asymmetrical GAA SNWT with $l_1 = 8$ nm and $l_2 = 12.5$ nm is chosen to compare with the equivalently symmetrical GAA SNWT with $l_1 = 10$ nm, as shown in Figure 1(e). It could be seen that two devices show almost the same $I_{\rm D}$-$V_{\rm G}$ characteristics at linear region.

With the proposed model, the impact of asymmetrical gate structure on the real gate control capability of GAA SNWTs can be investigated. As shown in Figure 1(f), the change of $L_{\rm eff}$ relative to l_1 is smaller than the change of l_2 relative to l_1 and almost nothing with l_1. It implies that the effective gate control capability of an asymmetrical GAA SNWTs is always between the symmetrical devices with gate lengths of l_1 and l_2. In other words, the short channel effect of the practically fabricated GAA SNWTs may not be degraded even though the apparent gate length l_1 aggressively scales down. However, that is at the cost of the increased bottom gate length l_2 and thus the parasitic capacitance. It will mislead the device engineer to overestimate the optimization result for the future GAA SNWT technology development. As a result, the inaccurate device model may be delivered to the IC designer. However, with the proposed model, the correction to proper gate length definition can be added to the commercial device model such as BSIM and thus make it more accurate.

Conclusion. In conclusion, an analytical effective gate length model was proposed for GAA SNWTs with asymmetrical gate structures. The model showed high accuracy when fitting to the simulated results. According to the model, the effective gate length may be longer than the apparent gate length and thus result in overestimated short channel effect controllability. The proposed model will provide proper theory guidance for the future optimization of GAA SNWTs.

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