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# Graphene-based vertical thin film transistors

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**Abstract** Vertical field effect transistors (VFETs), where the channel material is sandwiched between source-drain electrodes and the channel length is simply determined by its body thickness, have attracted considerable interest for high performance electronics owning to their intrinsic short channel length. To enable the effective gate modulation and current switching behavior, the electrode of conventional VFET is largely based on perforated metals, in which the gate electrical field could penetrate through. Recently, with the emerge of graphene, a new type of graphene based VFETs has been developed. With finite density of states and the weak electrostatic screening effect, graphene exhibits a field-tunable work-function and partial electrostatic transparency, it can thus function as an "active" contact with tunable graphene-channel junction, enabling entirely new transistor functions or higher device performance not previously possible. In this review, we discuss the research progresses of graphene-based VFET, including the its basic device structure, carrier transport mechanism, device performance and novel properties demonstrated.

**Keywords** graphene electrode, vertical transistors, thin film transistors, van der Waals heterostructures

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## 1 Introduction

Semiconductor devices have changed the world beyond anything that could have been imagined before [1–10]. Starting from the invention of the transfer resistor or transistor in 1947, the size of the transistor has been aggressively scaled, and till today, the physical length of a typical transistor is entering the sub-10 nm regime [10–19]. With decreasing channel length, the driving current and therefore the switching speed can be improved [2, 14, 20]. However, on the other hand, fabricating such short channel device is not an easy task, which typically involves sophisticated facilities and often high energy fabrication processes, and is becoming more and more difficult in the sub-10 or sub-5 nm regime [12, 16–18]. For example, fabricating short channel transistor requires extreme ultraviolet lithography (EUV) [13,18], high energy ion implementation [16,21] and rapid high temperature activation [22,23]. These complicated and often expensive fabrication processes pose a key challenge for the development and commercialization of various semiconductor devices, especially for macroelectronics (e.g., thin film transistors) that require the distribution of functional electronic components over large area [6, 23–25], where the high-resolution lithography or high-energy processes are difficult or too costly to apply.

To overcome this limitation, a new design of vertical field-effect transistor (VFET) has been developed [25–54], where a thin-film semiconductor body is simply sandwiched between the source and drain electrodes and the channel length is determined by its body thickness, as shown in Figures 1(a)–(d). This

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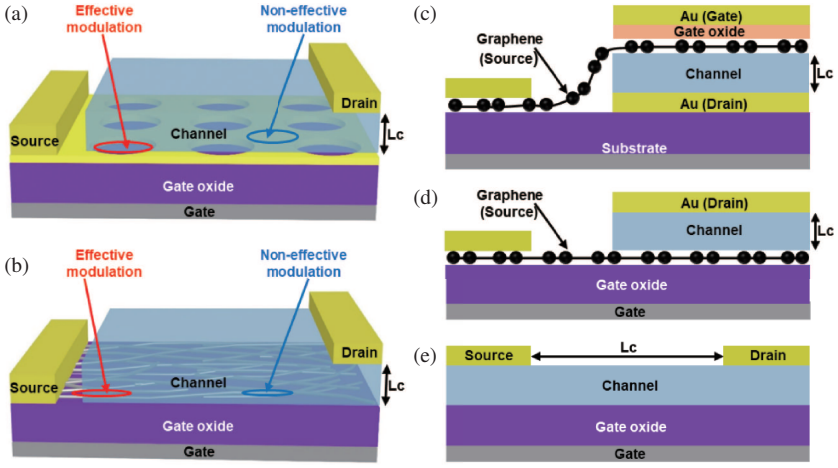


**Figure 1** (Color online) Three-dimensional perspective schematics of the perforated electrode based VFET (a) and nanowire based VFET (b), where the gate field could penetrate through the "holes" of the electrode, and hence modulate the conductivity of the channel material. Within this structure, the channel length is simply defined by the distance between source-drain electrodes. Schematic illustrations of the cross-sectional view of graphene-based top-gated VFET (c) and back-gated VFET (d). (e) A schematic of the conventional planar transistor, where the channel length is defined by the lithography resolution.

novel structure is in great contrast to the conventional planar transistors [18, 55, 56] (channel length defined by lithography resolution, as shown in Figure 1(e)), and high-resolution lithography is not necessary to achieve short channel length within VFET geometry [34, 36].

For functional operation of VFET, a key requirement is that one of the electrodes should be transparent to gate electric field to enable the effective modulation of carrier transport, which would otherwise cause electrostatic screening effect [25, 57]. Previous transparent contact electrodes are largely based on perforated metals [25] or nanostructure (such as silver nanowire, carbon nanotube) networks [49, 57, 58], as schematically illustrated in Figures 1(a) and (b). Within these device structures, the gate field could penetrate through the "holes" of the electrode, and hence modulate the conductivity of the channel material, leading to the ON and OFF states. To date, lots of achievements have been demonstrated using these structures, however, challenges still remain. From the fabrication point of view, the perforated metal electrode requires additional lithographic and/or etching techniques, and the aperture size has a significant impact on the switching characteristics of the device [25, 30]. Similarly, it is also hard to achieve uniform and low resistance metallic nanostructure networks using spin-coating techniques, and finite surface roughness may also impact the performance of VFET. For example, for Ag nanowire network electrode, the channel length of VFET (which is the semiconductor thickness) should be larger than the diameter (∼100 nm) of nanowire, to prevent the short circuit of VFET [57]. On the other hand, from the performance point of view, the perforated electrode based VFET cannot fully unlock the potential that vertical transistor may offer. As shown in Figures 1(a) and (b), although the gate electrical field could penetrate through the holes of the electrode, only the exposed "hole" channel area (labeled by red color in Figures 1(a) and (b)) can be modulated, where the real vertical channels (sandwiched between two metals, as highlighted by blue arrow in Figures 1(a) and (b)) are less impacted by the gate field and cannot be effectively switched between the ON and OFF states, greatly limiting the overall VFET performance.

With single atomic thickness, finite density of states (DOS) and weak screening effect, graphene exhibits a field-tunable work-function and partial electrostatic transparency [26, 42, 59–66]. It can therefore function as an 'active' contact in tunable graphene-semiconductor or graphene-insulator junction to enable entirely new possibilities for VFET application [42, 60, 61, 67–75]. Exploiting the tunable junction in the VFETs, new device structure, including tunneling transistors [47], field-effect transistors (FET) [41] or barristors [45] has been demonstrated with greatly improved ON/OFF ratio or current density.

In this review, we focus on the recent research progresses of graphene-based VFET. We will first start

with the device structures and the corresponding fabrication processes of graphene VFETs. Next, the device working mechanism and transport properties will be analyzed in detail. Finally, we will discuss some unique properties enabled by graphene VFETs, including large current density, high switching speed, flexibility, stability, and the novel vertical integration technique. We will finally conclude with a short perspective on the challenges and future developments of high performance VFETs.

## 2 Vertical device geometry, fabrication and transport mechanisms

The device structures of graphene-based vertical transistors are schematically illustrated in Figures 1(c) and (d). Within this device geometry, the carriers travel vertically between source and drain electrodes, where the current flow direction is in parallel with the gate electrical field direction [20]. This is in great contrast to the conventional planar transistor structure (Figure 1(e)) in which the current flow direction is always perpendicular with the gate electrical field direction [20]. Following this vertical geometry, two related but distinct device structures have been explored: top-gated VFET (Figure 1(c)) and back-gated VFET (Figure 1(d)). Within top-gated structure, bottom metal electrode is first directly deposited on substrate, followed by the integration of the channel material. Next, graphene is transferred on top of the channel material and then top gate stacks (including the gate dielectric and gate metal) are integrated. Although lots of VFET devices and circuits have been demonstrated following this top-gated structure, several fabrication difficulties remain. First, owing to the lack of dangling bonds on the pristine graphene surface, the deposition of high quality gate dielectric on graphene is hard to achieve. Although integration of a buffer layer (such as polymer or thin film metal seed layer) could partially alleviate this problem [76], doping to the underlayer graphene is hard to avoid. Secondly, it is usually difficult to achieve optimized contact between bottom electrode and semiconductor (especially for crystal semiconductors such as Si or III-V compounds) owing to the finite surface roughness of metal electrode and thus insufficient metal-semiconductor contact area [77]. Thirdly, the commonly used wet-transfer process of graphene [34] would involve undesired solution process on top of semiconductor, which may not be compatible with various water-sensitive channel materials such as organic or perovskite semiconductors.

To overcome these limitations, the back-gated VFET structure has been widely investigated [34,41,47]. Within this structure, graphene is first transferred or exfoliated on back-gate substrate with pre-fabricated gate electrode and gate dielectric (e.g., $p^{++}$ $Si/SiO_2$ substrate). Next, various channel materials can be integrated on top of graphene followed by deposition of top electrode, as shown in Figure 1(d). Compared to top-gated VFET, such back-gated structure ensures high quality gate dielectric and intimated metal contact (between top electrode and channel materials). However, the direct integration of channel material on top of graphene remains a critical challenge. The previous physical vapor deposition (PVD) or chemical vapor deposition (CVD) integration can usually compromise underlying monolayer delicate lattices and degrade/alter graphene electronic properties [78,79], hence low energy integration approaches (e.g., spin-coating, or van der Waals integration) should be applied within this structure [20,34,40,43,80–84].

With entire new VFET structure, the carrier transport mechanism is also different compared to conventional planar FET, and can be largely attributed to two different mechanisms: tunneling and thermionic emission [20]. Different from conventional tunneling field-effect transistors (TFET) which are relied on band-to-band tunneling (BTBT) mechanism [85], the operation of the tunneling VFET depends on the gate tunable density of states in graphene and hence the effective modulation of tunneling barrier height [43, 47]. The vertical TFET was first reported by sandwiching thin layer of BN (boron nitride) between two graphene electrodes, and the tunneling probability can be modulated by the gate induced barrier tuning, resulting in an ON/OFF ratio of ∼50 [47]. More importantly, the bottom graphene electrode only partially screens the gate electrical field because of its the low DOS and large quantum capacitance, resulting in the effective control of top graphene electrode and thus the tunneling coefficient, leading to unique negative resistance behavior [86], as shown in Figure 2(a).

The working mechanism could be further understood using band diagrams of a graphene-$WS_2$-graphene vertical transistor [43]. A negative gate voltage decreases the Fermi level of graphene, leading to the in-

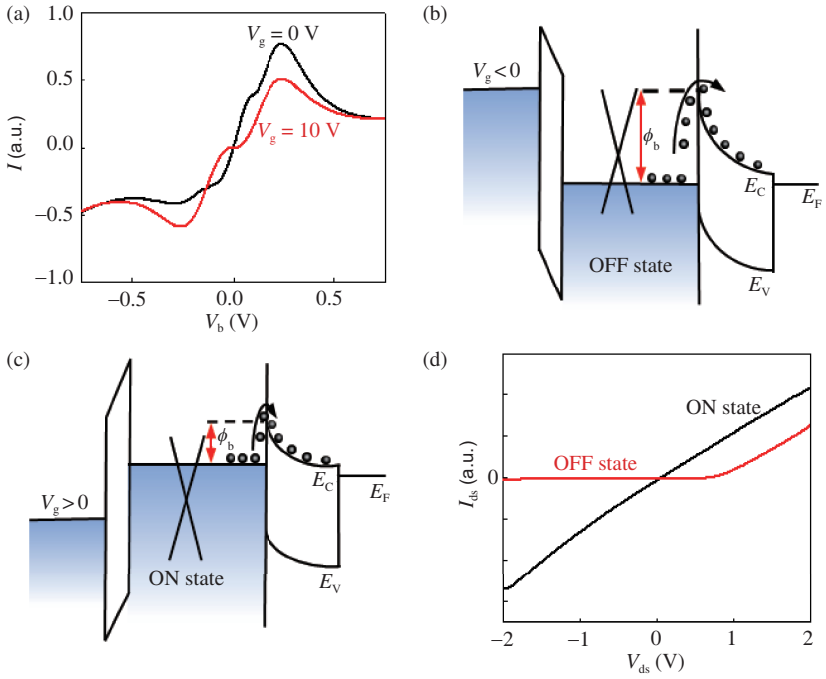


**Figure 2** (Color online) (a) The unique negative resistance characteristic of the graphene-BN-graphene tunneling vertical transistor [86] @Copyright 2013 Springer Nature. Band-diagram of the vertical thermionic transistor at OFF state (b) and ON state (c). A negative gate voltage increases the Schottky barrier height, resulting in the OFF state. On the other hand, when applying positive gate voltage to the transistor, the Schottky barrier is decreased and the device is at ON state. (d) The output characteristic of a typical thermionic vertical transistors.

crease of the tunneling barrier height, resulting in the OFF state of the VFET. On the other hand, a positive gate voltage shifts the Fermi level upward, resulting in the decrease of barrier height, and the device enters the ON state. Hence, such device yields relatively high ON/OFF ratio of $\sim 10^6$ owing to the possibility of switching between tunneling and thermionic transport regimes [43]. Furthermore, the current density of graphene-insulator-graphene tunneling VFETs is still relatively low for high performance devices. Replacing the top layer of graphene with highly doped silicon was demonstrated to increase the tunneling current owing to the much larger DOS of the highly doped silicon [32].

For the thermionic based VFET, the working mechanism can be explained by the band diagrams of a representative thermionic vertical transistor, or "barristor" [45] (Figure 2(b) and (c)). When graphene electrode is in contact with the semiconductor channel, Schottky barrier is formed between the two materials owning to their energy level difference. By modulating the graphene's work function through the gate electrical field, the resulting Schottky barrier height could also be changed, leading to the effective modulation of the overall carrier transport with large ON/OFF ratio. For example, for graphene-$MoS_2$ (n-type)-titanium VFET, a negative gate voltage would increase the work function of graphene, leading to much enhanced Schottky barrier height between graphene-$MoS_2$ heterojunction [20], as shown in Figure 2(b). Under this situation, the device behaves a Schottky diode with an obvious rectifying effect (the red curve of Figure 2(d)). On the other hand, a positive gate voltage would dope graphene with electrons and decrease the Schottky barrier height between graphene and n-type $MoS_2$, leading to linear output behavior and ON state of the device, as shown in Figure 2(c) and black curve of Figure 2(d). A series of vertical transistors have been reported following this working mechanism, with various channel semiconductors ranging from transition metal dichalcogenides (TMDCs) [33, 38, 40, 41], thin film organic semiconductors [34, 72], conventional amorphous metal oxide semiconductors [42, 87], as well as to bulk crystals [26, 32]. Furthermore, high ON/OFF ratio is always desired for VFET operation. To increase the ON/OFF ratio, one possible approach is to use large bandgap semiconductor (as the channel materials) to increase the OFF state barrier height, or using thicker materials (longer channel length) to increase the depletion width. However, under both situations, the ON state current could also be slightly decreased

and should be always considered when choosing the corrected material. Alternatively, the ON/OFF ratio could also be increased using thinner dielectric layer or high-$k$ dielectric to increase the gate controllability, leading to smaller OFF state current and higher ON state current.

We further note the transport mechanisms of graphene based VFET are different from the graphene based hot electron transistors (HETs), as have been demonstrated [88, 89]. For graphene based HETs, it is more like a conventional bipolar junction transistor (BJT) consisting collector, emitter and base regions. Within this structure, carriers (hot electrons) are directly injected/tunneled through the ultrathin dielectric between graphene and the emitter, where graphene here is used as the base region material owning to its atomic thin body thickness, leading to short transit time and a high gain while maintaining a low base series resistance. In contrast, graphene based VFET follows the conventional MOSFET structure, and is largely based on the electrostatic control of graphene work function and the resulting barrier height. There is no direct current flow from the gate electrode to graphene.

## 3 Unique properties of graphene based VFET

### 3.1 High driving current

With naturally short channel length simply defined by body thickness, the VFET could promise large driving current not previously possible using conventional planar device structure, where the channel length is dictated by the lithography resolution [34, 90]. For example, a $MoS_2$ VFET with channel area ~5 μm×5 μm could deliver high current of ~1 mA, corresponding to a current density over 5000 A/cm$^2$ [41]. In contrast, a conventional planar $MoS_2$ device (with channel length 5 μm and channel width 5 μm) only exhibits a current of ~10 μA (0.02 A/cm), around two orders of magnitude lower compared to the VFET [41]. Similar large driving current is also demonstrated using other channel materials such as $WSe_2$, where current density up to 3100 A/cm$^2$ was demonstrated within vertical device structure [33].

Such large driving current shows particular advantages in many applications where high resolution lithography is difficult to apply. For example, for display application (that requires components over large area) or flexible electronics on various soft substrates [4,5,23,91], conventional high-resolution lithography process is difficult to apply but large driving current is highly desired [44]. Another example is organic electronics that is incompatible with conventional lithography processes (degraded/dissolved in various solvents), hence shadow mask lithography is widely used in organic electronic research community, where the resolution is typical larger than 10 μm [92]. In contrast, using the graphene-based VFET structure, short channel device of ~100 nm has been demonstrated using various organic channel materials such as phenyl-C61-butyricacid methyl ester (PCBM), poly (3-hexylthiophene-2,5-diyl) (P3HT) [34]. For the vertical organic transistors, another structure benefit is the high stability, where the metal electron could act as a self-encapsulation for the semiconductor layer, protecting the delicate organic materials from impact of oxygen or water. This is in great contrast to the traditional planar device structures in which the channel material is exposed to air and easily degrades under ambient conditions [34].

### 3.2 High speed operation

High driving current is essential for the high-speed operation of the VFETs [41]. The design of vertical transistor opens a new pathway to high speed electronics without high resolution lithography. To this end, it is important to theoretically evaluate the scaling relationship between switching speed and device dimension, and experimentally measure its true speed value.

From the theory part, the speed of a given transistor can be roughly estimated through a simple relationship $\tau = RC$, where $\tau$ is the intrinsic delay, $R$ is the device resistance, and $C$ is the capacitance [20]. Detailed resistance $R$ and the corresponding speed can be theoretical analyzed using the resistance network model [26] (Figure 3(a)), where the total $R$ is composed by four different parts: $R_{gc}$, $R_{gs}$, $R_g$, and $R_v$. $R_{gc}$ is the graphene contact resistance, which varies from 50 to ~1000 Ω μm depending on

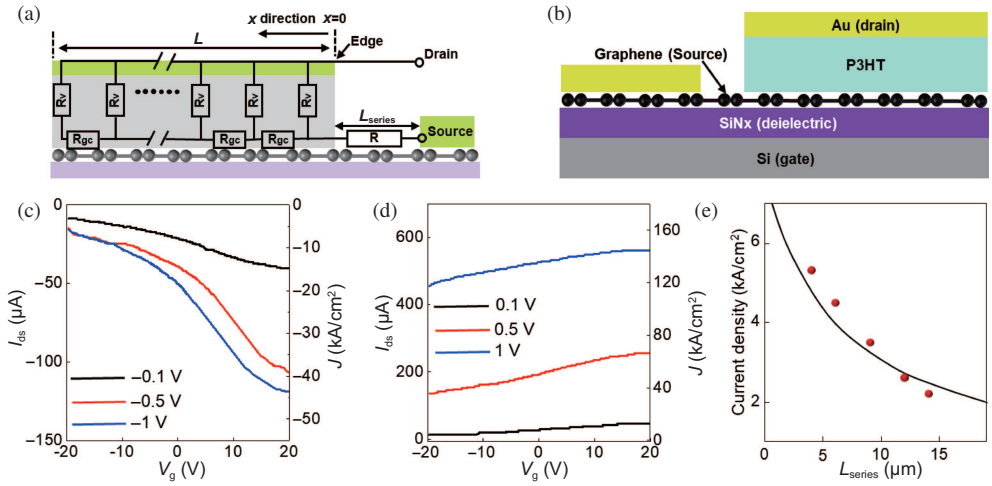


**Figure 3** (Color online) (a) Resistor network model of VFETs [26] @Copyright 2019 American Chemical Society. (b) A schematic of the cross-sectional view of the organic VFET device based on graphene-P3HT heterostructure [34] @Copyright 2015 American Chemical Society. Transfer characteristics of self-aligned graphene-InAs-metal VFET in negative bias region (c) and positive bias region (d) [26] @Copyright 2019 American Chemical Society. (e) The relationship between current density and the series graphene lengths in both experiment and calculated results [26] @Copyright 2019 American Chemical Society.

gate voltage and the contact metal used. $R_{gs}$ is series resistance between graphene contact and the semiconductor edge. $R_g$ is graphene channel resistance, which is 300 Ω/square for single layer graphene. $R_v$ is the total vertical resistance, including the junction resistance between graphene and semiconductor channel, the channel resistance, as well as the metal-semiconductor resistance. The $R_v$ is strongly related to doping carrier concentration of the channel material, because a highly conducting semiconductor $R_v$ ensures small contact resistance, channel resistance at the same time. To reduce the $R$ and increase the overall device speed, efforts should be put to minimize the above resistance values ($R_{gc}$, $R_{gs}$, $R_g$, $R_v$). For typical demonstrated VFETs [34, 41, 87], the $R_v$ dominates the overall device resistance, owning to the relatively low channel vertical conductivity compared to the highly conducting graphene electrode. Under this case, the graphene can be viewed as an ideal metal electrode with equal potential, where the bias voltage is totally applied on the semiconductor vertical direction [26]. Therefore, the current density and the speed of the VFET would not scale with the transistor geometry, suggesting the aggressive scaling (in lateral dimension) is not necessary for high speed transistors. For example, by increasing the device footprint, the overall current $I$ and the corresponding gate capacitance $C$ will be scaled up proportionally, with little change in the projected device speed. From this point view, the micrometer scale or even larger devices could ideally function as fast as nano-scale devices. This concept has been demonstrated using organic semiconductor P3HT as the channel material and direct shadow mask lithography with resolution of ∼100 μm [34], as shown in Figure 3(b). The measured cut-off frequency ($f_T$) is 0.4 MHz for this device, which compares well with nanoscale transistors using similar channel materials P3HT [93, 94]. However, the problems of organic high speed transistor are the relatively low vertical conductivity and low driving current (3.4 A/cm$^2$) [34]. By changing the channel materials to TMDCs such as $MoS_2$, higher current density over $10^3$ A/cm$^2$ has been demonstrated [41], suggesting a highest cut-off frequency of ∼1 GHz using equation $f_T = g_m/2\pi C$, where $g_m$ is the device transconductance.

To further increase the switching speed, reducing the $R_v$ is essential. To this end, the use of high mobility materials (such as InAs thin film) as the channel material is beneficial [26], where the single crystal structure and the small bandgap (∼0.36 eV) of InAs could provide small metal contact resistance as well as low channel vertical resistance at the same time. Together, large ON current density over 45 kA/cm$^2$ and 142 kA/cm$^2$ has been demonstrated at reverse and forward bias voltages [26], as shown in Figures 3(c) and (d), with a projected cut-off frequency of ∼100 GHz. With such highly conducting channel, the bias voltage potential will have a signification drop on the graphene electrode. Hence, smaller $R_g$ and $R_{gs}$ are needed to further improve the speed of VFET. The reduction of $R_g$ could be achieved

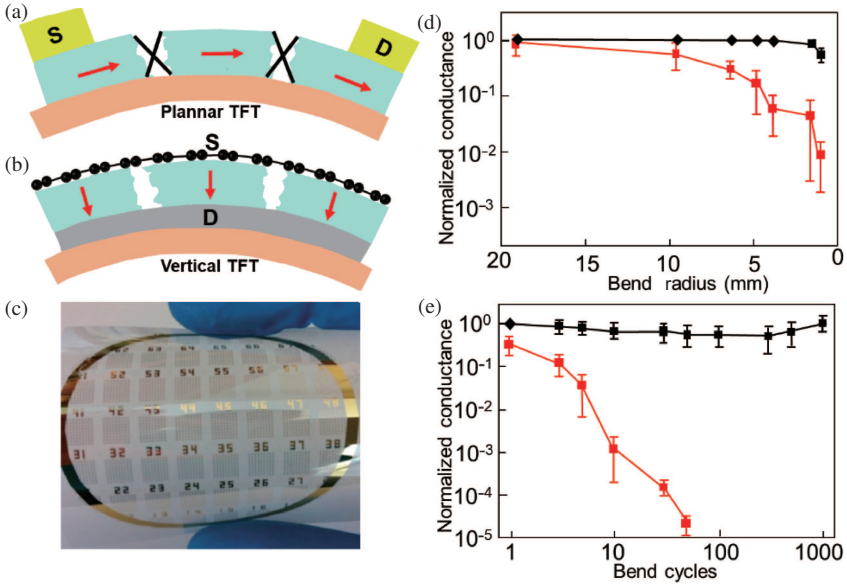


**Figure 4** (Color online) (a) A schematic of conventional planar structure with the brittle material as the channel, where the channel crack could result in overall device failure [87] @Copyright 2014 American Chemical Society. (b) A schematic of the VFET with the brittle material as the channel, and the vertical current transport is largely unaffected by the in-plane crack in the brittle films [87] @Copyright 2014 American Chemical Society. (c) Image of IGZO-graphene VFETs integrated on a PET flexible substrate [87] @Copyright 2014 American Chemical Society. (d) Normalized conductance of planar IGZO FET (red) and IGZO-graphene VFETs (black) under various bending radius [87] @Copyright 2014 American Chemical Society. (e) Normalized conductance of the planar IGZO structure (red) and vertical IGZO-graphene structure (black) at various bending cycles, showing better robustness of the VFET architecture [87] @Copyright 2014 American Chemical Society.

by using multilayer graphene or highly doped graphene [95,96], but both of which could sacrifice its gate tunability and the overall ON/OFF ratio. On the other hand, the minimized $R_{gs}$ can be achieved using a self-alignment method to shorten the series graphene lengths and to further improve the overall current density (Figure 3(e)) [26].

### 3.3 High flexibility

Flexibility is an important feature for future flexible, wearable, injectable or implantable devices [4,97,98]. Previous approaches to achieve high flexibility largely rely on the use of ultrathin channel materials to reduce the applied strain [43] or by using intrinsically flexible materials such as organic polymers [4]. Within the unique VFET structure, a new flexible transistor mechanism could be developed, where typical non-flexible or brittle material could also be used as the channel material for high performance flexible electronics [87]. As shown in the schematics in Figure 4(a), when brittle semiconductor is mechanically bended or stretched, any small in-plane crack/slip of channel can severely degrade the lateral charge transport in conventional planar structure. In contrast, within the VFET structure, the vertical current transport (out-of-plane) is largely unaffected by the in-plane crack in the brittle films (Figure 4(b)). It has been demonstrated that indium-galliam-zinc-oxide (IGZO) VFET is much more robust than the planar counterpart, and the current level shows little change even up to 1000 bending cycles [87] (Figures 4(c)–(e)). Similarly, a $WS_2$ based VFET was reported by fabricating the vertical heterostructures on a flexible polyethylene terephthalate (PET) film [43], demonstrating high flexible VFET with stable electrical characteristic under bending.

### 3.4 Scalability and 3D integration

Scalability is another important issue for the practical application of the graphene base VFETs. From electrode point of view, large area CVD grown graphene is highly desired for scalable application [42], however the undesired wet-transfer process could introduce potential contamination during the fabrication

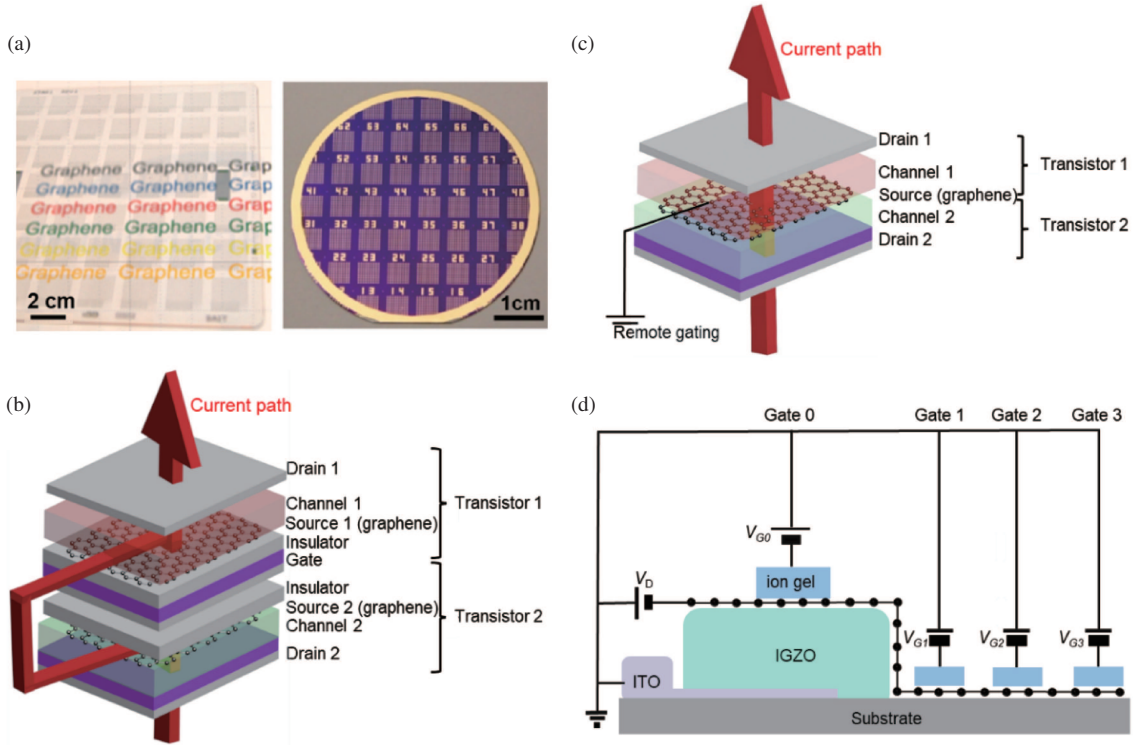


**Figure 5** (Color online) (a) Photograph of vertical transistors integrated on a 6-inch transparent glass wafer with 2000 devices (left) [42] @Copyright 2013 American Chemical Society. Photograph of vertical transistors integrated on a 2-inch wafer with an array of 1620 devices (right) [87] @Copyright 2014 American Chemical Society. (b) Schematic illustration of current path between vertically integrated transistors in the conventional stacking approach [75] @Copyright 2019 American Chemical Society. (c) Schematic illustration of current path between vertically integrated transistors in the remote gating approach [75] @Copyright 2019 American Chemical Society. (d) Schematic of the cross section of a remote gating vertical-Schottky barrier transistor with gate electrodes positioned at different locations [75] @Copyright 2019 American Chemical Society.

process. This is especially true for the bottom-gated VFET structure (Figure 1(c)) where graphene top surface is directly in contact with the semiconductor, and any polymer residues (such as PMMA (polymethyl methacrylate)) could seriously impact the overall device performance. On the other hand, from the semiconductor point of view, the typical mechanically exfoliated TMDC channel is clearly not suitable for scalable VFETs. Although lots of achievements have been made to grow large area of TMDC materials, they are more focused on monolayer or bilayer materials that are not suitable for VFET application owing to strong direct tunneling effect within such short channel length (∼1 nm) [33, 38, 41]. From this point of view, conventional oxide or organic semiconductor thin films (that can be deposited or spin-coated) are more suitable for scalable fabrication [34, 36, 42, 48, 99]. For example, wafer scale integration of VFETs based on IGZO asymmetric junctions is demonstrated on a transparent 6 inch glass substrate (Figure 5(a) (left)), with a maximum current ON/OFF ratio up to $10^6$ over 2000 devices under ambient conditions [42]. Furthermore, logic functions such as inverter, NOR, and NAND are demonstrated using top-gated IGZO VFETs on a 2 inch wafer [87], as shown in Figure 5(a) (right).

Despite conventional scalable method by fabricating more parallel devices, the vertical transistors can be integrated in the vertical direction by stacking different devices layer by layer, representing the device-level 3D integration [100, 101]. This kind of vertical stacking of unit devices does not consume additional space besides what is needed for a single device at the bottom [75, 102]. For example, a complementary inverter with a voltage gain of ∼1.7 was created by vertically stacking the layered materials of graphene, $Bi_2Sr_2Co_2O_8$ (p-channel), graphene, $MoS_2$ (n-channel) and a metal thin film in sequence [41]. However, integrating multiple transistors in vertical direction remains challenging, because the bottom gate electrical field cannot modulate too many layers and additional gate electrode (as well as gate dielectric) is required. In this case, the current between the different stacked transistors will not flow

vertically in a straight line (as shown in Figure 5(b)), instead it would pass the dielectric layer through complex interconnect holes [75]. On the other hand, as have been previously noted, the integration of dielectric layer on graphene or on existing bottom transistor is still challenging. To solve this problem, a remote modulation strategy is reported recently [75]. By placing an ion-gel gate laterally away from the graphene-semiconductor junction, the work function of graphene (under the junction) can be tuned, resulting in the effective modulation of the vertical transistors even without any dielectric layer on the junction area, as shown in Figures 5(c) and (d). Within this geometry, a series of transistors can be vertically stacked (without dielectric in between) and the current can straightly flow between the vertical channels without a bypass, opening up the possibility of 3D integration of VFETs at the device-level (Figure 5(c)). Besides, it is also noted that other dielectrics such as high-$k$ $Al_2O_3$ also can be used for remote gating, but the tunability could be greatly reduced owning to the smaller gate capacitance and weaker gate electrostatic coupling [75].

## 4 Outlook

Although initial studies of graphene based VFET have revealed exciting opportunities, many challenges remain. In particular, with a dangling-bond free surface, the integration of high-quality material (insulator, metal, semiconductor) on top of graphene is hard to realize without damaging the delicate monolayer lattice. On the other hand, integration of graphene on other materials is also not an easy task, where the transfer size, yield, wrinkles, surface contamination of graphene and interfacial air bubbles (with any given substrate) represent notable technical challenges that could severely limit the device reliability and scalability. To this end, the recent developed vdW integration of 3D semiconductors on graphene could alleviate this problem, however, the finite semiconductor surface roughness could impact the overall charge transport and the intimate vdW contact between graphene and single crystal materials deserves further attentions.

Besides the integration challenges, the scaling of VFETs is also seldomly investigated, and it is still unknown for the thickness scaling limit of channel material. Within ultra-short vertical channel length, vertical short-channel effect, vertical Fermi level pinning effect and the carrier saturation effect could play important roles in high performance VFETs. This requires integrated efforts from not only the electrical engineers for experimental designs and process developments, but also theorists for constructing new vertical device model that is intrinsically different from conventional transistor structure. Despite these and other challenges, the naturally short channel length and vertical carrier transport within VFET could enable semiconductor devices with novel functions for future electronics.

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