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Fully coupled electrothermal simulation of resistive random access memory (RRAM) array

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Dear editor,

Resistive random access memory (RRAM) is a promising candidate for next generation memory technology [1] and the rapid progress in the three-dimensional (3D) integration technology facilitates the design of highly integrated and miniaturized RRAM devices [2]. However, the ever-growing storage density does lead to thermal crosstalk a critical issue as the temperature rise in the victim may induce rupture of conductive filament (CF) and reliability degradation.

The electrothermal model given in [3] is employed to describe the electrothermal process in RRAM array. A parallel simulator based on a hybrid finite volume-finite element (FVFE) method and parallel processing technique is developed to numerically study the electrothermal performance in large-scale arrays. Here, a double level parallel scheme base on domain decomposition method (DDM) and the J parallel adaptive unstructured mesh applications infrastructure (JAUMIN) [4] is implemented. Using the developed simulator, the electrothermal properties of a proposed cross-gate vertical RRAM (CGVRRAM) array are investigated.

Architecture of the proposed CGVRRAM array. The vertical architecture is one of the most widely used RRAM array structure, and the schematics of a conventional vertical RRAM array and its cell are illustrated in Figures 1(a) and (b). As indicated in [5], thermal crosstalk effects in vertical RRAM array do affect its performance. To improve the thermal management in vertical RRAM array, a novel RRAM (VRRAM) array architecture is proposed as shown in Figure 1(d). We name it CGVRRAM array. Moreover, it also can be seen that compared with the traditional vertical array structure, the proposed one possesses higher integration density.

During the operation of the proposed CGVRRAM, the states of word lines, bit lines, and selectors determine the memory chain, while the cross-gate lines are used to select the cell in the chain. If there is no cross-gate line chosen, the poly-Si layers can serve as current channels [6]. On the contrary, if one cross-gate line is selected, the channel under it will be TURN OFF, and the current flows through the adjacent cell.

Electrothermal model. The electrothermal process taken place in an RRAM consists of ion migration, current transport, and thermal conduction [3]. The electrical simulation can be performed by solving the ion transport equation and current continuity equation, i.e.,

$$\nabla \cdot (\mu(T) n_D \boldsymbol{E} - D(T) \nabla n_D) = \frac{\partial n_D}{\partial t} + RG, \quad (1)$$

$$\nabla \cdot (\sigma(T) \nabla V) = 0, \quad (2)$$

where V is the voltage, T is the local temperature, $\boldsymbol{E} = -\nabla V$ is the electric field, $\mu(T)$ is the temperature-dependent mobility, $D(T)$ is the

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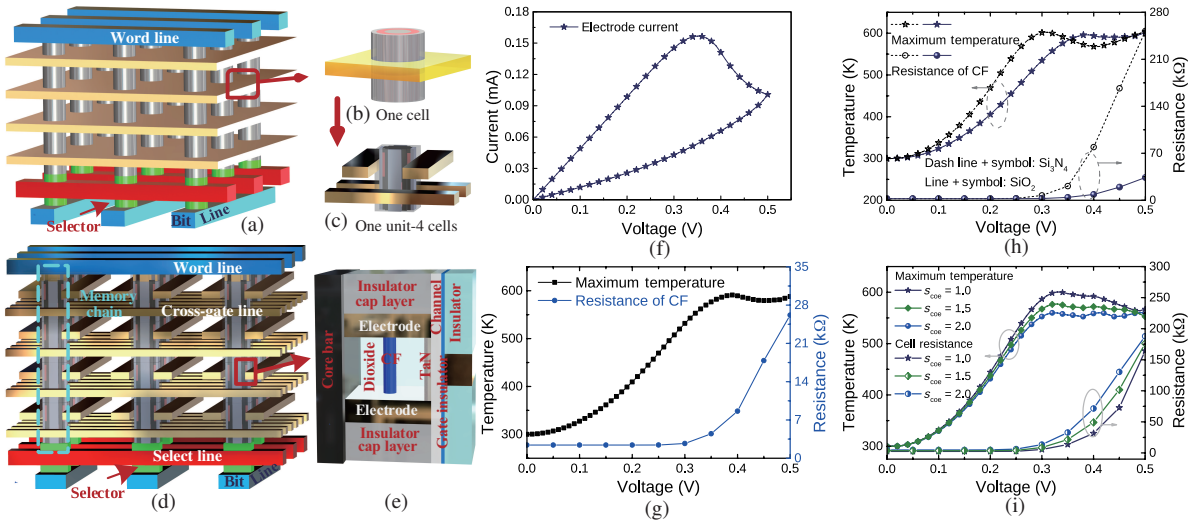

Figure 1 (Color online) (a) and (b) schematics of conventional VRRAM array and its cell; (c) 4-cell unit, (d) array, and (e) cell structures of the proposed CGVRRAM; (f) electrode current and (g) the maximum temperature and reset resistance of CGVRRAM cell as a function of biasing voltage; (h) the maximum temperatures and cell resistances of CGVRRAM unit as a function of biasing voltage; (i) the maximum temperature and cell resistance of programmed cells as a function of biasing voltage.

ion diffusion coefficient, n_D is the ion concentration, and RG is the generation/recombination rate. $\sigma(T)$ is temperature-dependent electrical conductivity [3].

The thermal simulation is conducted by solving the governing equation as

$$\rho c_p(T)\frac{\partial T}{\partial t} = \nabla\cdot(\kappa(T)\nabla T) + Q, \qquad (3)$$

where $c_p(T)$ and $\kappa(T)$ are the temperature-dependent heat capacity and thermal conductivity of the materials, respectively [7].

Numerical scheme. In the simulations, the geometric model, as well as input information, is loaded at first and then the J parallel adaptive unstructured mesh applications infrastructure (JAUMIN) evenly divides the whole model into distributed patches using the Metis software package. After that, each patch is assigned to one process according to the inherent workload distribution scheme. To balance the workloads and dynamically minimize the number of successive subdomains allocated to each process, message passing interface (MPI) parallel programming scheme is utilized. On each patch, the ion transport equation and current continuity equation are solved and subsequently, the heat generation rate is calculated as the source in heat conduction equation. During this process, the FEM is employed to discretize the current continuity and heat conduction equations, while the FVFE-SG method is implemented for solving the ion migration governing equation [8]. A HYPER-PCG solver is utilized to solve the system matrix equation on each patch. The details of numerical strategy are given in Appendix A.

Electrothermal simulation of CGVRRAM array. As stated above, a novel high-density CGVRRAM array is proposed in this study. By virtue of the in-house developed simulator, its electrothermal characteristics are examined in this section. In the simulations, the poly-Si channel in OFF state is modeled as low electrical conductivity silicon. Dimensional parameters are given in Appendix B.

The reset process of a CGVRRAM cell is activated by applying a triangular voltage pulse with 1 V/s ramp and 0.5 V amplitude to the top boundary of the poly-Si channel. The I-V curve of the simulated cell is plotted in Figure 1(f), with the maximum temperature and cell resistance shown in Figure 1(g). It is found that the electrode current increases first and then decreases with the increasing biasing voltage. This is mainly because the CF is switching to high resistance state as the voltage increases. Moreover, when the biasing voltage of 0.5 V is applied, a 27-fold increase in the cell resistance can be achieved.

Then, the electrothermal characteristics of the CGVRRAM unit shown in Figure 1(c) are simulated. Two cases are considered, in which SiO_2 and Si_3N_4 are used as dielectric components (i.e., core bar, insulator caps, and substrate material), respectively. In Figure 1(h), the maximum temperature and cell resistance of the activated cell of CGVRRAM unit as a function of biasing voltage are plotted. It is evident that by replacing SiO_2 dielectric components with Si_3N_4 ones, the maximum temperature becomes increasing faster,

thereby leading to a higher growth rate in cell resistance. In one sense, this implies that the implementation of Si_3N_4 dielectric components is beneficial to low power applications.

After that, the electrothermal characterization of the CGVRRAM array composed of 18 units (i.e., 72 cells) is conducted. As technology scaling is always desirable owing to lower cost for unit storage space, the electrothermal characteristics of scaled CGVRRAM arrays with Si_3N_4 dielectric components are examined. It is assumed that the scaling factor sweeps from 1.0 to 2.0. In the simulations, only one cell is activated by applying a triangular voltage pulse with 1 V/s ramp and 0.5 V amplitude. In Figure 1(i), the maximum temperature and cell resistance of the activated cells as a function of biasing voltage are plotted. It is observed that the maximum temperature in the scaled array is lower while the resistance of RRAM cell shows opposite trend. This changing trend can be explained as follows.

(1) The initial cell resistance can be calculated by

$$R_{\text{cell}} = \frac{1}{\sigma} \cdot \frac{h_{cf}}{2\pi r_{cf}^2}. \tag{4}$$

The value of $\frac{h_{cf}}{2\pi r_{cf}^2}$ is enlarged during scaling down which leads to the cell resistance to increase. For example, the initial cell resistance for $s_{\text{coe}} = 1.0$ is 2.41 kΩ but it increases to 3.61 and 4.82 kΩ for $s_{\text{coe}} = 1.5$ and $s_{\text{coe}} = 2.0$.

(2) The increase in cell resistance of the scaled RRAM cell will reduce the heat generation rate which could lead to the decrease in temperature.

(3) The resistance ratios between cells with different scaling factors go down with the biasing voltage. For example, the initial resistance ratio between cells with $s_{\text{coe}} = 2.0$ and $s_{\text{coe}} = 1.0$ is 2, but it is 1.14 when the biasing voltage is increased to 0.5 V. That is mainly because of the higher temperature in cell with $s_{\text{coe}} = 1.0$.

More simulation results can be found in Appendixes B and C.

Conclusion. In this study, an in-house developed parallel simulator was adopted to study the electrothermal characteristics of RRAM arrays. In the simulator, a hybrid numerical strategy based on finite volume method, finite element method and Scharfetter-Gummel method was implemented for numerical discretization, and a JAUMIN and DDM based double-level scheme was employed for parallel simulation. A novel CGVRRAM architecture was proposed and its electrothermal characteristics were studied using the internal simulator. The simulation results indicated that the proposed design performed excellent in both electrical performance and thermal management. In particular, the Si_3N_4 dielectric components, introduced to replace SiO_2 ones, were potential for improving thermal management and enabling low power operation of the CGVRRAMs.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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