• LETTER •



June 2020, Vol. 63 169401:1–169401:3 https://doi.org/10.1007/s11432-019-9842-3

A photomemory by selective-assembling hybrid porphyrin-silicon nanowire field-effect transistor

Gong CHEN¹, Bocheng YU², Xiaokang LI¹, Xiaoqiao DONG³, Xiaoyan XU¹, Zhihong LI², Ru HUANG¹ & Ming LI^{1*}

¹Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics,

Peking University, Beijing 100871, China;

²National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Peking University, Beijing 100871, China; ³Faculty of Information Technology, Beijing University of Technology, Beijing 100124, China

Received 25 February 2019/Revised 17 March 2019/Accepted 25 March 2019/Published online 12 February 2020

Citation Chen G, Yu B C, Li X K, et al. A photomemory by selective-assembling hybrid porphyrin-silicon nanowire field-effect transistor. Sci China Inf Sci, 2020, 63(6): 169401, https://doi.org/10.1007/s11432-019-9842-3

Dear editor,

Recently, the integration of photosensitive material and electronic nanodevice has been the center of attention with Internet of things (IoT) technology development [1-3]. The immobilization of such photoactive molecules on the semiconductor surface was necessarily adopted to employ their photoelectric characteristics which can be observed in the solution. Porphyrin-based hybrid transistors have emerged as promising candidates for photonic sensing application due to the confirmed photo-induced charge transfer (PCT) behavior between porphyrin molecules and electronic platforms [4]. Silicon nanowire is also considered as an ideal configuration to detect stimulus due to large suface-to-volume ratio and excellent transport property [5]. However, most of existing porphyrin/Si nanowire transistor showed transient light response only when the illumination occurred [6-8], and yet an entire photoelectric microsystem is constructed by not only photonic sensor but also other memory counterpart. In this case, an extra number of memory devices were necessary to keep the transformed electrical information recorded, which makes the whole system redundant and complex.

In this study, we successfully proposed and fabricated a porphyrin/si hybrid photomemory by a

novel selective-assembling silicon nanowire transistor. Thanks to the hydrophobicity difference between SiO_2 and Si_3N_4 , the enrichment of water soluble porphyrin onto nanowire surface can be achieved, and a wealth of porphyrin layer is also the key to realize photomemory because molecular orbits in a wealthy and ordered porphyrin layer tend to split so that PCT behavior can be more easily triggered from nanowire to porphyrin's redox energy level. It is demonstrated that our photomemory could store charge under illumination and also dissociate it by applying electrical field, which can be ignored in a conventional hybrid nanowire device since its molecular orbits in porphyrin layer can hardly split.

Experiment. From the very beginning, p-type (1 0 0) silicon wafer was used. For the selectiveassembling porphyrin-silicon nanowire field-effect transistor (PSNFET), LPCVD $SiO_2/Si_3N_4/SiO_2$ stack was firstly implemented as the isolation layer with thicknesses of 10/150/7 nm. For the control sample, only an oxide layer was deposited. Then, a poly-si layer of 25 nm was deposited as the channel material, and the nanowire widths were defined by electron beam lithography (EBL) ranging from 40 to 450 nm. The source and drain regions were patterned by optical lithography and followed by heavy As⁺ implantation with energy and dosage of

 $^{\ ^*} Corresponding \ author \ (email: \ liming.ime@pku.edu.cn)$



Figure 1 (Color online) (a) SEM image of our fabricated selective-assembling PSNFET; (b) the cross-sectional schematics of PSNFET along (left) and perpendicular (right) to nanowire channel with TPPS selectively assembled; (c) electrical program and erase characteristics of the SA PSNFET assembled with 1 and 10 μ M TPPS (left), the bare SA PSNFET (middle) and the control sample (right); (d) the light programming and electrical erasing speed of the novel SA PSNFET with 1 μ M TPPS functionalization (left and middle). The retention of light programmed SA PSNFET with 100 nm width and 1 μ M TPPS (right).

20 KeV and 5×10^{13} cm⁻², respectively. The rapid thermal processing (RTP) process was performed at 1050°C afterwards. Aluminum/titanium stack was adopted as metal connection and pad material. Last but not least, a Si₃N₄ layer of 400 nm with a assembling window was necessary to expose the nanowire channel as well as avoid porphyrin coated on passivation. Considering the possible contamination of porphyrin to metal connection, the Al/Ti pads were designed far away from the channel region. At last, the back gate electrode was formed to apply V_g so that nanowire channel can be modulated. Herein, the scanning electron microscope (SEM) image of our fabricated PSNFET was illustrated in Figure 1(a).

To get the complete porphyrin/silicon hybrid device, the water solution of meso-tetra (4sulfonatophenyl) porphyrin (TPPS) was dropped on the surface of chips. After 24-hour drying at 20% humidity and 25°C, TPPS molecules were coated onto the hydrophilic surface through hydrogen bonds and π - π stacking interaction. For the novel selective-assembling PSNFETs, owing to great difference in hydrophobicity between nanowire and surrounding area, TPPS solution was only adhered to the surface of nanowire, as shown in Figure 1(b). In contrast, TPPS molecules randomly aggregated in the whole assembling window of the control group because the adhesion of TPPS to nanowire could not distinguish itself from the surrounding oxides.

Results and discussion. The electrical memory characteristics of the novel selective-assembling (SA) PSNFETs was confirmed in Figure 1(c). At higher molarity of TPPS, the memory window of the selective-assembling PSNFET was enlarged from 15.6 to 31.3 V under $V_{\rm PGM} = 20$ V and $V_{\rm ERS} = -20$ V both applied to the back gate. To avoid the controversy about Fowler-Nordheim (FN) injection into the nitride stack beneath the selective-assembling PSNFET, the bare device without TPPS functionalization was programmed and erased under the same conditions. The V_T window of bare selective-assembling PSNFET is negligible compared to TPPS assembled devices. On the other hand, as the control group, conventional PSNFET modified with TPPS showed smaller V_T window than the selective-assembling PSNFET even with higher molarity TPPS of 100 μ M.

Base on the electrical memory results above, we analyzed that the plausibly mechanism of programing and erasing behavior of the SA PSNFET come from the transfer behavior of electrons between valence band in nanowire and lowest unoccupied molecular orbits (LUMO) in porphyrin LUMO in SA PSNFET tended to laver [9]. split into several molecular orbits due to its enhanced orbital coupling effect originated from enriched and ordered porphyrin molecule arrangement, which was equivalent to the band gap narrowing of porphyrin and made transfer behavior easier to happen for electrons. Once the porphyrin is positively or negatively charged by back gate electrical field, the threshold voltage of nanowire will be pushed to shift correspondingly.

Light has always been regarded as another effective manner to modulate the states of porphyrin. Here, besides the electrical memory behavior, it was observed in Figure 1(d) that the novel SA PSNFET with top porphyrin layer could be programmed by light and erased by electric field over a quite large V_T range. The results convinced us that the occurrence of illumination played the same role with applying the positive programing back gate voltage. When the incident light appeared, photoelectrons were generated in nanowires, they could be easily injected into TPPS to occupy LUMO and trapped as the fixed negative charges to induce V_T positive shift, just like the way the electrical programing worked. Furthermore, the fixed negative charges may enhance the surface scattering so that device mobility tend to degrade, which can be observed in the on-state current dropping. It is also demonstrated that the light programmed V_T can maintain for a relatively long term within reasonable V_T dropping.

We proposed and fabricated a Conclusion. novel selective-assembling silicon nanowire transistor with an enriched top porphyrin floating layer by CMOS technology. The key advantage of our novel device originated from the hydrophobic isolating design, resulting in a unique photomemory property that the incident light can act as a programing signal to keep the photo-induced electrons stored in the unoccupied molecular orbits of enriched porphyrin layer and the negative charge inside TPPS layer can also be erased by applying electrical field. The special photomemory characteristics of our selective-assembling PSNFET provides a hopeful possibility and open a new mind for simplifying and innovating the photonic sensor device design in the future IoT application.

Acknowledgements This work was partly supported by National Key Research and Development Plan of China (Grant No. 2016YFA0200504), National Natural Science Foundation of China (Grant No. 61421005) and 111 Project (Grant No. B18001).

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