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Complementary tunneling transistors based on WSe_2/SnS_2 van der Waals heterostructure

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Dear editor,

Two-dimensional (2D) semiconductors have emerged as one of the most promising material candidates for next-generation electronic devices [1]. Owing to the broad range of bandgap diversity and the pristine interface, 2D semiconductors have triggered tremendous research interest for various device applications, especially in tunnel field-effect transistors (TFETs) [2–4]. To date, most of the experimental demonstrations of 2D-based TFETs mainly focus on either n-type or p-type device, and are realized in different material systems, which is not preferred for highly-integrated circuits. In [5], both n-type and p-type TFETs based on the reconfigured structure and black phosphorus (BP) material have been realized through electrical modulation of carrier types of the source and the drain. However, due to the inherent small band gap of BP, the leakage current and on/off current ratio of devices are unsatisfactory. Complementary TFETs based on the same 2D material system with superior performance are still in urgent need. Moreover, most of the 2D TFET reports focus on the reduction of effective tunnel barrier height for drive current enhancement, while few studies have been reported for the improvement of output characteristics. Some typical features in the output curves of TFETs, such as super-linear onset phenomenon, could degrade the dynamic property and static noise margin of digital circuits [6]. Therefore, both transfer and output characteristics should be considered for the complementary TFET design.

Taking into consideration of transfer and output characteristics, both n-type and p-type TFETs are designed and experimentally demonstrated based on the WSe_2/SnS_2 van der Waals heterostructure. The type-II band alignment of WSe_2/SnS_2 heterostructure with reduced effective tunnel barrier height is beneficial for high tunnel current, and the thicknesses of WSe_2 and SnS_2 in n-TFET and p-TFET are optimized separately to suppress the super-linear onset in output curves. The fabricated complementary TFETs show on/off current ratio of 10^4, which is much higher than that of the previously reported BP TFETs [5]. The tunneling mechanism of fabricated devices is also confirmed by the temperature-dependence characteristics.

Device structure and design principle. Figures 1(a) and (b) show the schematic structures of the bottom-gated complementary TFETs based on van der Waals heterostructure in this study. The SiO_2 and highly-doped Si are used as the gate dielectric and the bottom gate, respectively. The channel layer is designed to be under the source layer so that the channel potential could be controlled by the bottom gate with the better gate controllability. Besides, taking into consideration of both transfer and output characteristics, the 2D-based complementary TFETs are designed according to the following principles. Take the p-TFET for example.

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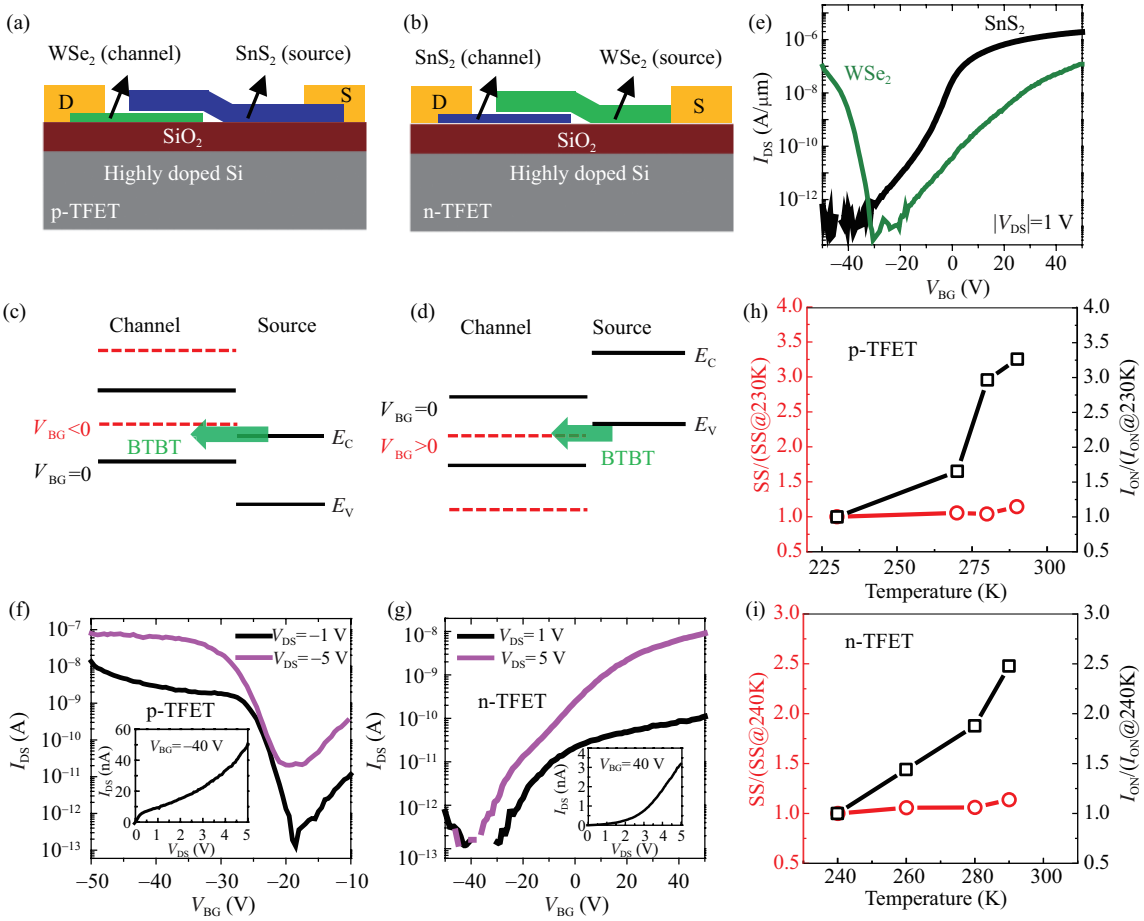

Figure 1 (Color online) The schematic structures of p-TFET (a) and n-TFET (b). The band alignment of p-TFET (c) and n-TFET (d) in the off-state and on-state. The transfer characteristics of the WSe_2 and SnS_2 FET (e). The measured transfer characteristics of p-TFET (f) and n-TFET (g) at room temperature; (Inset) the corresponding output characteristics. Temperature-dependence characteristics of the p-TFET (h) and n-TFET (i).

The band alignment of the van der Waals heterostructure is designed to be type-II, in which the valence band of the channel layer is below the conduction band of the source layer, so that the effective tunnel barrier height could be considerably reduced for larger tunnel current. The working principle of p-TFET is shown in Figure 1(c). In the off-state, there is no tunneling window for band-to-band tunneling (BTBT) process. When a negative bias is applied on the bottom gate, the valence band energy (E_V) of the channel layer begins to be higher than the conduction band energy (E_C) of the source layer, and the BTBT process across the source/channel heterojunction will take place. Among all kinds of 2D semiconductors, WSe_2/SnS_2 van der Waals heterostructure with theoretically 0.18 eV stands out as the superior material system for TFET [7]. The WSe_2 transistors usually exhibit ambipolar characteristics and thus the WSe_2 could be used as the p-type channel layer of p-TFET, while the SnS_2 exhibits n-type characteristics and thus can be used as the n-type source layer of p-TFET [8], as shown in Figure 1(e).

Moreover, according to our previous results in [6], the source density of states (DOS) should be enlarged to improve the subthreshold slope of TFET, and the relatively low DOS of the channel material is preferred for the better output curves with suppressed super-linear onset voltage of TFET. Since the DOS of 2D semiconductors is sensitive to the layer thickness [9], the SnS_2 thickness is designed to be relatively large (~50 nm) for the relatively large source DOS, while the thickness of WSe_2 channel layer is less than 10 nm for the low DOS.

The design principles of n-type TFET is similar to that of p-type TFET. In n-TFET, SnS_2 serve as the channel layer with the relatively small thickness, and WSe_2 serve as the source layer with the relatively large thickness.

Results and discussions. Figures 1(f) and (g) show the measured typical transfer characteristics of fabricated p-type TFET and n-type TFET at

room temperature. Insets are the corresponding output characteristics. For p-TFET, the results are obtained by applying the bias on WSe_2 contact, with SnS_2 contact grounded. For n-TFET, the SnS_2 contact is biased, with WSe_2 contact grounded. The on-state current (I_{ON}) of fabricated p-TFET and n-TFET based on WSe_2/SnS_2 van der Waals heterostructure are about 80 and 10 nA, respectively. The on/off current ratio of the devices are about 10^4, which is much higher than the reported TFETs based on the BP material [5], showing the superiority of WSe_2/SnS_2 van der Waals heterostructure for tunneling devices. Since the complementary TFETs are fabricated using the bottom-gated structure with 300 nm-thick SiO_2, the subthreshold slope (SS) is relatively large and can be optimized by further reducing the gate oxide thickness or incorporating with high-κ dielectrics. Besides, it can be seen that the super linear onset phenomenon still exists in the output characteristics, even with the optimized thickness of the source layer and channel layer in our work. It could be partially attributed to the Schottky contact of 2D semiconductors and can be further improved by reducing the Schottky contact resistance in the future work.

In order to further verify the tunneling mechanism of the complementary TFETs based on WSe_2/SnS_2 van der Waals heterostructure, the temperature dependence of I_{ON} and SS are studied. As shown in Figures 1(h) and (i), I_{ON} shows the positive dependence on temperature and SS changes little with temperature, exhibiting the typical features of BTBT operation mechanism. The weak dependence of SS on temperature also indicates the good quality of tunneling junction with few traps in the devices of this study.

Conclusion. Taking into consideration of transfer and output characteristics, both n-type and p-type TFETs are realized based on the designed WSe_2/SnS_2 van der Waals heterostructure. The fabricated complementary TFETs show on/off current ratio of 10^4 which is much higher than that of previous reports. The tunneling mechanism is also experimentally confirmed. This study shows the great potential of 2D semiconductors for low-power complementary tunneling devices.

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