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Influence of an ALD TiN capping layer on the PBTI characteristics of n-FinFET with ALD HfO_2/TiN-capping/TiAl gate stacks

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Dear editor,

High k/metal gate (HKMG) stacks with fully gate-last processing have become the primary solution for sub-22-nm volume manufacturing with the development of complementary oxide semiconductor (CMOS) technology [1]. In the HKMG stack, titanium nitride (TiN) is observed to play an important role as a work-function metal and an HK capping layer. Instead of the physical vapor deposition of TiN, the atomic layer deposition (ALD) of TiN has been extensively applied owing to its improved step coverage and filling capability with respect to the nanoscale trenches, particularly in case of nonplanar devices such as fin field-effect transistors (FinFETs). As a work-function metal electrode, thick ALD TiN layers have been reported to reduce the gate leakage and improve the reliability of the bias temperature instability (BTI) [2]. However, few studies have reported the impact of ultrathin ALD TiN as a capping layer for HK dielectrics with respect to the electrical characteristics of the advanced HKMG CMOS devices, particularly in case of a positive BTI (PBTI) [3, 4]. This study intends to investigate the impact of an ultrathin ALD TiN capping layer on the PBTI of n-type FinFETs; we prepared two n-type FinFET samples with and without an ALD TiN capping layer on a HfO_2 HK dielectric. Further, the electrical measurements were performed under a constant electrical field and fixed gate bias (V_g) stresses, and energy dispersive spectrometry (EDS) analysis was conducted to verify the physical origin of the defects in the HK material.

Experiment. The spacer image transfer technique was applied for fin formation in the HKMG n-FinFET process. After the completion of the poly-open chemical mechanical polishing (CMP) process and the elimination of the dummy gate material, the HKMG stack was deposited in the gate trench after conducting a standard cleaning process. Further, a 6-Å interfacial layer was grown by chemical oxidation, followed by the deposition of a 2.6-nm ALD HfO_2 layer and post-deposition annealing at 450°C for 15 s in nitrogen, for fabricating the HKMG stack. Subsequently, the ALD TiAl/TiN/W gate stacks were deposited. Two samples were produced. For one sample, a 1.4-nm ALD TiN layer was inserted between the HfO_2 and

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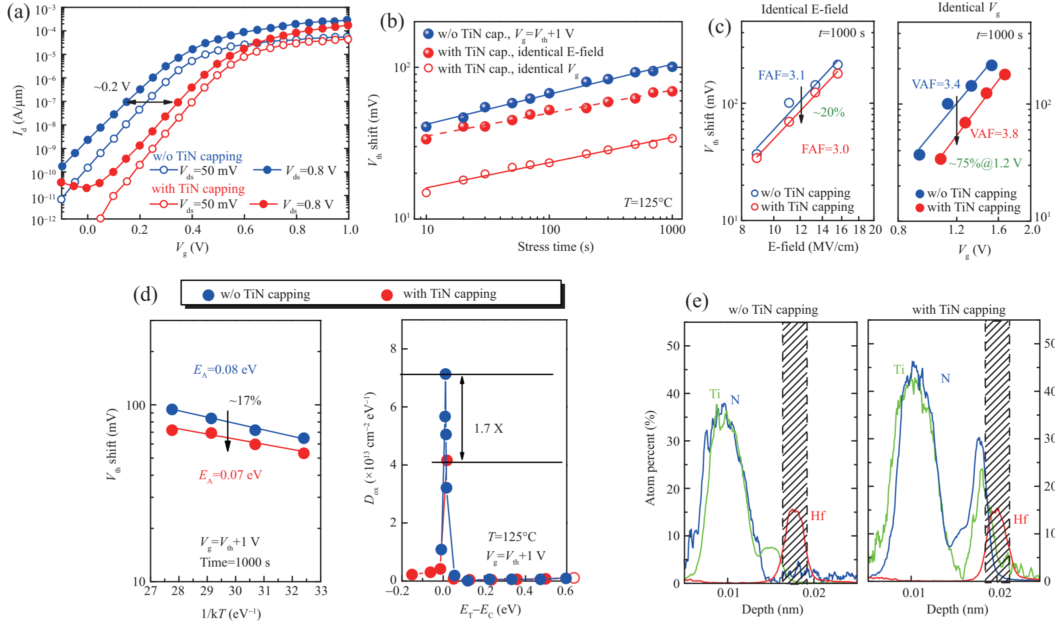

Figure 1 (Color online) (a) I_d-V_g curves of n-FinFETs with (red) and without (blue) an ALD TiN capping layer. (b) The V_{th} shift and stress time for devices with (red) and without (blue) an ALD TiN capping layer at 125°C over 1000 s. (c) V_{th} shift of n-FinFETs with and without an ALD TiN capping layer over 1000 s. (d) The V_{th} shift as a function of temperature with 1 V over-drive voltage stress at 1000 s. The energy distribution of traps in the HK layer for V_{th} + 1 V at 1000 s and 125°C. (e) EDS data for n-FinFETs without and with an ALD TiN capping layer.

TiAl layers as the capping layer. Further, the final gate lengths of the two n-FinFETs ranged from 27 to 500 nm with a typical value of 33 nm. For simplicity, the sample without the TiN capping layer will be referred to as the control sample, whereas the sample with the TiN capping layer will be referred to as the capping sample.

Results and discussion. Electrical measurements were conducted using a Keysight B1500A analysis system at both room temperature and high temperature. As depicted in Figure 1(a), V_{th} of the n-FinFETs with a typical gate length of 33 nm increased by approximately 0.2 V with the insertion of the ALD TiN capping layer. This trend can be attributed to an increase in the effective work-function because of the insertion of the mid-gap metal TiN and the prevention of an Al-diffusion-induced dipole at the HK/MG interfacee [5]. Owing to the excellent gate controllability of the tri-gate structure, the two samples also exhibited the short channel effect with subthreshold swings (SSs) of 91 and 88 mV/dec and drain-induced barrier-lowering values of 70 and 51 mV, respectively.

As depicted in Figure 1(b), a gate bias stress with an over-drive of 1 V (V_g = V_{th} + 1 V) was initially applied to the control sample at 125°C (blue). Further, a shift of approximately 40 mV can be observed in case of V_{th} due to the presence of PBTI stress at 10 s. For comparison, the identical V_g stress was applied to the capping sample, exhibiting a small V_{th} shift of approximately 15 mV at 10 s. By considering different initial V_{th} values, a constant electric field stress was applied to both the control sample and the capping sample. With respect to the identical electric field stress, the V_{th} shift of the capping sample was smaller than that of the control sample, indicating fewer traps in the capping sample when compared with that in the control sample.

In Figure 1(c), the V_{th} shift was plotted as a function of the electric field stress and V_g stress at 125°C for 1000 s. For an electric field stress ranging from 0.9 to 16 MV/cm, the field acceleration factors of the two samples were observed to be similar, and the PBTI V_{th} shift was reduced by approximately 20% in case of the ALD TiN capping layer. With respect to the V_g stress, the voltage acceleration factor of the capping sample was observed to be slightly larger when compared with that of the control sample but still comparable. Furthermore, the V_{th} shift of the capping sample was approximately 75% lower than that of the control sample for a V_g stress of 1.2 V.

The activation energy (E_A) for electron trapping under PBTI stress was determined by varying the test temperatures (85°C, 105°C, 125°C, and 145°C), as depicted in Figure 1(d). Herein, a constant electric field stress was applied with a 1-V gate over-drive voltage. The PBTI values

for the capping layer sample are approximately 17% lower than those of the control sample. The determined E_{A} values of both samples were less than 0.1 eV, indicating that the PBTI degradation was dominated by the pre-existing traps instead of the generated traps [6]. Furthermore, the energy distribution of the traps in the HfO_2 layer was also extracted from the recovery characteristics (not shown here) [7], as presented in Figure 1(d). The trap density peaks for the two samples were located near the edge of the conduction band (E_{c}). The peak trap density of the control sample was approximately 70% larger when compared with that of the capping sample. Such pre-existing traps near E_{c} were generally assumed to be induced by the neutral oxygen vacancies (V_{O}^{0}) in the HK materials [8]. Therefore, it can be inferred that the passivation mechanisms occur in case of oxygen vacancies due to the insertion of the ALD TiN capping layer.

Line-scanning EDS was performed to determine the origin of PBTI improvement in case of the capping sample. The results are presented in Figure 1(e), where the HK/MG interface was defined as the half-density location of hafnium. The nitrogen density in the HK layer of the capping sample was considerably higher than that of the control sample due to nitrogen diffusion from the ALD TiN capping layer. The diffused nitrogen in the HK layer can bind with the dangling Si bonds around the oxygen vacancies, annihilating the pre-existing traps in the HK layer [9].

Conclusion. Herein, the impact of the ALD TiN capping layer on the PBTI performance of n-type FinFETs was experimentally investigated. The activation energy and trap density were compared, indicating that the pre-existing traps dominated the PBTI degradation in both the samples; however, due to the nitrogen passivation effect, the capping sample exhibited better PBTI performance. This study provides comprehensive physical reference data for ensuring PBTI improvements in future CMOS technology.

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