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A novel tunnel FET design through hybrid modulation with optimized subthreshold characteristics and high drive capability

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Dear editor,

As CMOS technology scaling down, the reduction of supply voltage and power consumption becomes extremely difficult due to the subthreshold swing (SS) limitation (60 mV/dec) at room temperature. Tunnel FET (TFET) with band-to-band tunneling (BTBT) mechanism is regarded as one of the most promising emerging low-power devices due to its sub-60 mV/dec SS and ultra-low off-current ($I_{\rm OFF}$), especially for Si TFET [1–4]. To date, a lot of research and efforts have been made on optimizing the subthreshold characteristics of TFETs. Since the minimum subthreshold swing ($\rm SS_{min}$) for TFET is determined by the electric field at tunnel junction when BTBT just turns on, by the novel device designs or the process optimization, TFETs with sub-60mV/dec $\rm SS_{min}$ have already been experimentally demonstrated [5–7]. However, the SS tends to degrade with the increasing $V_{\rm GS}$ for traditional TFET, which is found to be fundamentally caused by the degraded BTBT generation rate increment with increasing gate voltage [8]. Hence, the most reported TFETs can only achieve steep SS within low drive current level, which may induce the large average SS ($\rm SS_{avg}$) and also low drive capability. Therefore, device optimization strategy of TFET for simultaneously achieving the steep $\rm SS_{min}$ and suppressing SS degradation is in ample necessity for TFETs.

In this study, a novel junction-modulated hetero-layer TFET (JHL-TFET) is proposed and investigated. Based on the hybrid effect of adaptive bandgap engineering and junction depleted-modulation, compared with traditional TFET, JHL-TFET can achieve the steeper $\rm SS_{min}$ and the suppressed SS degradation behavior simultaneously. The device performance of JHL-TFET has been comprehensively studied to evaluate its potential for ultra-low application.

Device structure and operation principle. Figure 1(a) gives the schematic and sectional view of the proposed JHL-TFET. Compared with traditional TFET, the JHL-TFET features a striped-shaped gate stretched into the stacked source region with relatively larger bandgap material as the upper layer and relatively smaller bandgap material as the underlying layer. The thicknesses of the upper layer and underlying layer are defined as $T_{\rm upper}$ and $T_{\rm underlying}$, respectively. Besides, the large bandgap material is also used as the channel and drain materials to ensure low off-current. The length of the striped gate stretched into the source region is defined as L_f and the width of the striped gate is defined as W_f.

By using Synopsys TCAD Sentaurus simulation tools, device simulation was carried out to investi-

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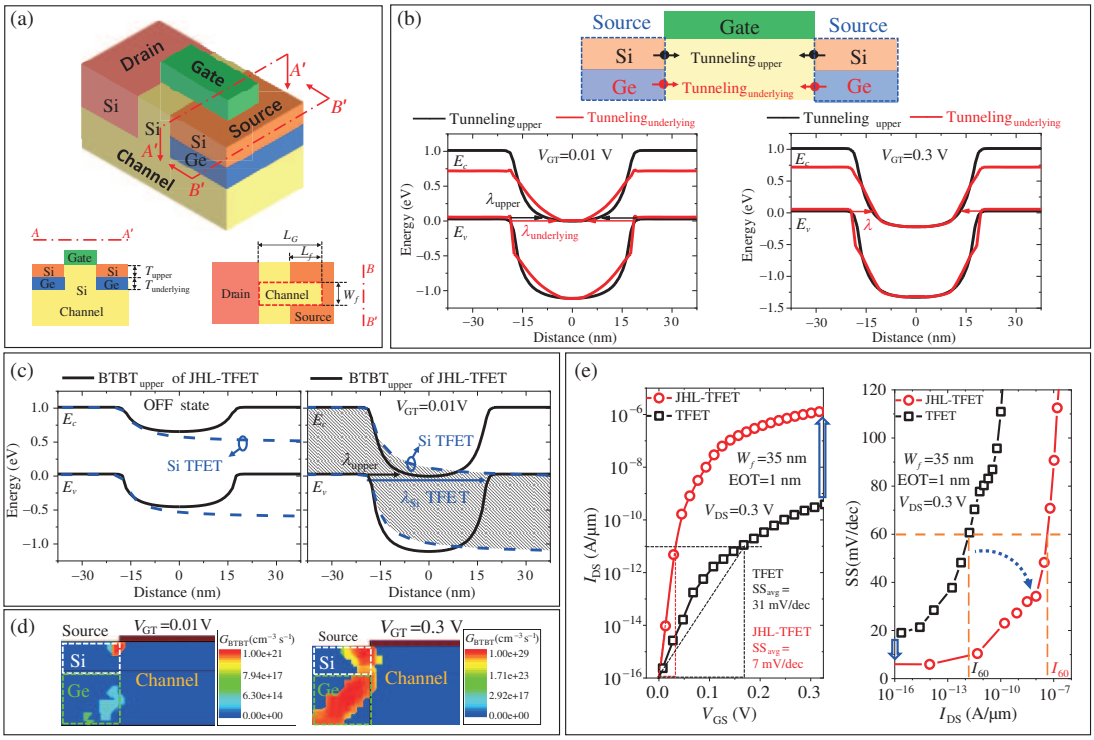

Figure 1 (Color online) (a) The schematic view of the proposed JHL-TFET, the sectional view of the proposed device perpendicular to the channel (AA') direction, the section view of the proposed device along channel (BB') direction; (b) the cross-sectional schematic of tunneling components in source region along AA' direction in Figure 1(a), and simulated energy band along tunneling direction for $\mathrm{BTBT_{upper}}$ and $\mathrm{BTBT_{underlying}}$ of Si-Ge JHL-TFET when $V_{\mathrm{GT}} = 0.01$ and 0.3 V; (c) simulated surface energy bands of traditional Si TFET and energy band for $\mathrm{BTBT_{upper}}$ of the Si-Ge JHL-TFET for off-state and $V_{\mathrm{GT}} = 0.01$ V; (d) simulated G_{BTBT} in source region of Si-Ge JHL-TFET for $V_{\mathrm{GT}} = 0.01$ and 0.3 V; (e) simulated transfer curves and SS of Si-Ge JHL-TFET and traditional Si TFET of the same footprint.

gate the device operation principles. The dynamic nonlocal path band-to-band tunneling model and the Shockley-Read-Hall recombination model were included. The A_{Kane} and B_{Kane} parameters used in the dynamic nonlocal path band-to-band tunneling model are calibrated with the experimental results [4]. For simulated JHL-TFET and traditional TFET, the gate oxide thickness and gate length (L_G) are 1 nm and 100 nm, the doping concentration of P+ source and P− channel are 1×10^{20} and 5×10^{14} cm^{-3}, and the doping concentration of drain is 1×10^{18} cm^{-3} for suppressing the ambipolar effect. Besides, for JHL-TFET, the L_f is 35 nm, and Si and Ge materials are used as the upper layer and underlying layer materials respectively in the stacked source structure for the device simulation. Moreover, T_{upper} is 5 nm and $T_{\mathrm{underlying}}$ is 10 nm.

To investigate the operation principle, Figure 1(b) shows the simulated adaptive bandgap design of the JHL-TFET. It can be seen that there are two kinds of tunneling processes in the source tunneling junction. One is tunneling from source upper layer to channel (defined as $\mathrm{BTBT_{upper}}$) and the other is tunneling from source underlying layer to channel (defined as $\mathrm{BTBT_{underlying}}$). During the switching process, because of the strong electrostatic control of gate, the tunneling barrier width of $\mathrm{BTBT_{upper}}$ (λ_{upper}) is much smaller than the tunneling barrier width of $\mathrm{BTBT_{underlying}}$ ($\lambda_{\mathrm{underlying}}$) at low gate voltage. As the gate voltage further increases, the $\lambda_{\mathrm{underlying}}$ will further reduce and become close to the λ_{upper}. Since the bandgap and carrier effective mass of underlying layer are smaller than those of upper layer, the BTBT generation rate (G_{BTBT}) of underlying layer can be increased significantly, which provides the remarkable tunneling probability enhancement with increasing gate voltage.

For JHL-TFET, since the $\mathrm{BTBT_{upper}}$ is dominant for total current when the device just turns on, the $\mathrm{SS_{min}}$ of JHL-TFET is determined by the characteristics of $\mathrm{BTBT_{upper}}$. Figure 1(c) shows the simulated energy bands of $\mathrm{BTBT_{upper}}$ for Si-Ge JHL-TFET and surface energy bands for traditional TFET when devices are in the off-state and just turned on. For Si-Ge JHL-TFET, due to the narrow gate width of the striped gate, the channel area between two P+ stacked source region ($W_f \times L_f$) can be fully depleted by the side

source junctions, which is called as the junction depleted-modulation effect [4, 5]. As a result, Si-Ge JHL-TFET can achieve higher energy band than traditional TFET when devices are in the off-state. As gate voltage further increases, the BTBT switches on when the conduction band of channel is lower than the valence band of source for both devices. Si-Ge JHL-TFET can achieve the sharper band bending at source/channel interface than traditional TFET due to the modulated tunneling junction, which can induce the steeper SS_{min} [4].

For JHL-TFET, to further confirm the contributions of the $BTBT_{underlying}$ to the total current during switching process, Figure 1(d) extracts the simulated G_{BTBT} in the sectional view of source region for Si-Ge JHL-TFET. It can be seen that, for low gate voltage, the tunneling process mainly occurs in the surface. As the gate voltage increases, the G_{BTBT} of underlying layer becomes comparable to that of upper layer in Si-Ge JHL-TFET, and achieving a kind of adaptive G_{BTBT} replenishment behavior in the proposed device. Therefore, the remarkable tunnel probability enhancement of $BTBT_{underlying}$ with increasing gate voltage can suppress the SS degradation behavior in traditional TFET. Moreover, the appropriate T_{upper} may result in the better electrostatics of the $BTBT_{underlying}$ for larger G_{BTBT} increment and thus better sub-threshold behavior while maintaining low off-current (I_{OFF}) [9]. Besides, the adaptive G_{BTBT} replenishment of $BTBT_{underlying}$ can boost drain current of the JHL-TFET at high gate voltage, which can effectively address the issue of the low drive capability of traditional TFET.

Device characteristics. The simulated transfer curves and subthreshold characteristics of Si-Ge JHL-TFET and traditional Si TFET of the same footprint are shown in Figure 1(e). It can be seen that because the steeper SS_{min} (reduced from 19.2 to 6.0 mV/dec) and the suppressed SS degradation behavior can be simultaneously achieved in Si-Ge JHL-TFET, compared with traditional Si TFET, the SS_{avg} of Si-Ge JHL-TFET (SS value extracted extracted over 4 decades of I_{DS} from I_{OFF}) has been reduced from 33.1 to 6.3 mV/dec. Besides, Si-Ge JHL-TFET can achieve four decades I_{60} improvement compared with traditional Si TFET (I_{60} defined as the drain current corresponding to SS = 60 mV/dec). Moreover, since the underlying layer material (Ge) has the smaller bandgap than the upper layer material (Si), the Si-Ge JHL-TFET exhibits significantly improved I_{ON} than traditional Si TFET due to the adaptive replenishment current of underlying layer at high V_{GS}. Besides, the I_{OFF} of Si-Ge JHL-TFET remains the same level as Si TFET due to the larger bandgap of the upper layer. Therefore, the simulation results indicate that compared with traditional Si TFET, the Si-Ge JHL-TFET shows significantly improved driver capability and subthreshold characteristics without I_{OFF} degradation.

Conclusion. We have proposed and investigated a novel JHL-TFET design. Modulated by the hybrid effect of adaptive bandgap engineering and junction depleted-modulation, the Si-Ge JHL-TFET exhibits significant improvement for the subthreshold characteristics and the drive capability than traditional Si TFET while maintaining low I_{OFF}, which indicates its great potential for the ultra-low power applications.

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