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Vertical SnS_2/Si heterostructure for tunnel diodes

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Abstract Tunneling FET (TFET) is considered as one of the most promising low-power electronic devices, however, suffers from the low drive current. Heterostructure TFET with low effective tunnel barrier height based on traditional 3D materials can obtain large tunnel current but deteriorated off-state current induced by the lattice mismatch. van der Waals heterostructure TFET based on 2D materials can obtain dangling-bond-free interface for suppressed off-state current but face the challenge of controllable and stable doping technology. As the critical building block of the TFET, tunnel diode based on the 2D/3D heterostructure is proposed in this study and experimentally demonstrated. Combination of the pristine interface of 2D materials and matured doping technology in the traditional 3D bulk materials, tunnel diodes based on the 2D/3D heterostructures are expected to realize low leakage current and high on current simultaneously, showing great potential in low-power electronics. The N^+ SnS_2/P^+ Si heterostructure with effective tunnel barrier of 0.17 eV theoretically is considered for the first time and selected as the optimal material platform for tunnel diodes. The N^+ SnS_2/P^+ Si tunnel diode demonstrated experimentally shows the high current density of 1 $\mu A/\mu m^2$, which is the highest one among the reported tunnel diodes based on the 2D/group IV materials. The tunneling current is also confirmed by low-temperature measurements. This study shows the great potential of the 2D/3D heterostructure for low-power tunneling devices.

Keywords 2D/3D heterostructure, SnS_2/Si, tunnel barrier, tunnel diode, energy-efficient

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1 Introduction

For conventional metal-oxide-semiconductor field-effect transistor (MOSFET), power consumption has become the biggest bottleneck for further scaling down. The key obstacle is from the fundamental thermionic limitation of the subthreshold slope (SS) in MOSFET [1, 2]. Tunneling FET (TFET), which can break the above limit and possess the subthermionic subthreshold slope due to its band-to-band tunneling (BTBT) mechanism, has become one of the most promising candidates for future low-power applications, especially for low standby-power application [1, 2]. However, the tunneling current is relatively low for silicon-based TFETs due to the relatively large tunnel barrier height. Heterostructure TFETs based on traditional bulk materials, such as SiGe, InAs, GaAs, have been widely investigated due to the relatively low effective tunnel barrier height for high tunneling efficiency and high tunneling current [3, 4]. However, the lattice mismatch at the heterostructure interface will introduce interface states which may cause the trap-assisted tunneling current and deteriorate the off-state current and on/off current ratio [4]. Recently, TFETs based on van der Waals heterostructures composed of two-dimensional (2D) materials have gained tremendous research interest due to their dangling-bond-free interfaces [5–11].

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The dangling-bond-free interface could mitigate the parasitic trap-assisted tunneling induced by interface states. However, for 2D TFETs, the doping technology in 2D materials is very challenging and the controllable and stable doping is difficult to obtain for the source or drain [5]. Since the doping technology in traditional 3D bulk materials is highly matured compared with that in 2D materials [5], the heterostructure TFET combining a 2D material as the channel and a 3D bulk material as the source is supposed to obtain highly doped source and pristine interface of the heterostructure simultaneously [2]. The 2D material as the channel will enhance the gate controllability for steeper subthreshold slope. The interface between the 2D material and 3D material is still van der Waals interacted without lattice matching for low off-state current [2, 6]. The presence of the van der Waals gap at the interface also enables the ultra-sharp doping profile of the source tunnel junction for high tunneling field and thus high tunneling current [2, 12]. Moreover, the contact resistance of the 3D materials to metal can also be reduced compared with that of the 2D materials to metal [13]. Consequently, TFETs based on the 2D/3D heterostructures are expected to realize low leakage current and high on current simultaneously, and show the great potential in low-power electronics. Tunnel diode based on the 2D/3D heterostructures is the critical building block of the above TFET. However, only a few experimental studies have been reported regarding the tunnel diodes or devices based on the 2D/3D heterostructures. P^+ MoS_2/N^+ GaN, N^+ MoS_2/P^+ Ge and N^+ MoS_2/P^+ Si tunnel diodes have been reported [2, 12, 14]. However, the band alignment of these 2D/3D heterostructures is either type I (P^+ MoS_2/N^+ GaN) or type II with relatively high effective tunnel barrier height (0.4 eV in N^+ MoS_2/P^+ Ge and 0.78 eV in N^+ MoS_2/P^+ Si), leading to the limited tunneling current densities. Therefore, performance improvement of 2D/3D tunnel diodes or devices with high current density are still in urgent need.

In this study, the N^+ SnS_2/P^+ Si heterostructure with effective tunnel barrier height of 0.17 eV theoretically is considered for the first time and selected as the optimal material platform for tunnel diode. The fabricated N^+ SnS_2/P^+ Si tunnel diode shows the current density of 1 $\mu A/\mu m^2$, which is the highest one among the reported tunnel diodes based on the 2D/group IV materials. The tunneling current is also confirmed by low-temperature measurements. This study shows the great potential of the 2D/3D heterostructure for low-power tunneling devices.

2 Device physics and fabrication

2.1 Device physics

Figure 1 shows the schematic structure and top view of the vertical 2D/3D tunnel diode in this study. The 3D material is highly doped and the 2D material is designed to be the opposite type to form the P/N heterojunction. The 2D material sheet is designed above the 3D material for the future transistor fabrication. Considering that most of the 2D materials show n-type characteristics due to the structural defects [15], the doping of 3D material is designed to be p-type in this study. The band alignment of the 2D/3D heterostructure is designed to be type-II, in which the conduction band of the n-type 2D material layer is above the valence band of the p-type 3D material. The heterostructure of type-II band alignment with low effective tunnel barrier height enables the high tunneling efficiency and thus the high tunneling current. According to the band structures of various 2D semiconductors and 3D bulk materials, since the electronic affinity of SnS_2 is relatively large compared to other 2D semiconductors and relatively low effective tunnel barrier height can be formed for the SnS_2/Si heterostructure, N^+ SnS_2/P^+ Si heterostructure stands out as the superior material platform for tunnel diode. Figure 2 illustrates the operation mechanism of the vertical N^+ SnS_2/P^+ Si tunnel diode. Figure 2(a) illustrates the bandgaps and electronic affinities of Si and SnS_2, and the tunnel barrier height is determined to be 0.17 eV theoretically [16]. Figure 2(b) illustrates the band diagram of the N^+ SnS_2/P^+ Si tunnel diode in the equilibrium state. Electrons in the valence band of the p-type Si cannot tunnel into the conduction band of the n-type SnS_2 layer since there is no tunneling window. When the negative voltage is applied to the Si contact, the tunnel diode is biased in the reverse region. The conduction band energy (E_C) of the n-type SnS_2 begins to be lower than the valence band energy (E_V) of the p-type Si, and the tunneling

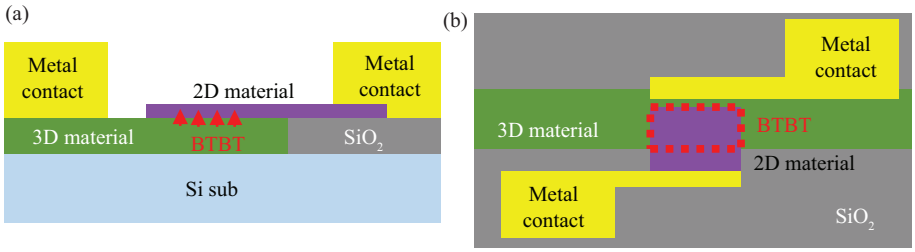

Figure 1 (Color online) (a) Schematic view of the vertical 2D/3D tunnel diode. Vertical tunneling occurs across the overlap region between the 2D material and the 3D material. (b) Top view of the vertical 2D/3D tunnel diode.

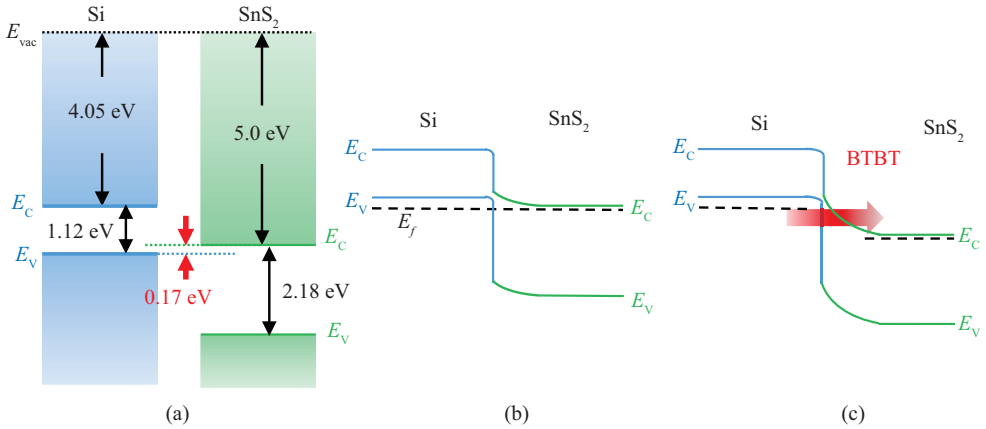

Figure 2 (Color online) The band diagram of the N^+ SnS_2/P^+ Si tunnel diode. (a) The bandgaps and electronic affinities of Si and SnS_2; (b) the equilibrium state; (c) the working state-reverse bias region.

current across the SnS_2/Si heterostructure dominates and increases accordingly.

2.2 Device fabrication

The details of the process used to fabricate the vertical SnS_2/Si tunnel diode are illustrated in Figure 3. The lightly-doped Si⟨100⟩ substrate is firstly prepared, and the impurity $BF_2{}^+$ is implanted successively with doping density of 1×10^{21} cm^{-3}. After lithography, Si is selectively dry-etched to form trenches. Then SiO_2 is formed by chemical vapor deposition (CVD) and is treated by chemical mechanical polishing (CMP) to flatten the surface. The wafer is then treated in hydrofluoric acid (HF) in order to remove the residual SiO_2 and the native oxide on the Si surface. Then the SnS_2 sheet is mechanically exfoliated onto the Si substrate within a short time interval to minimum the growth of native oxide and thus the 2D/3D heterostructure is formed. Metal contacts were sequentially defined by electron beam lithography, electron beam evaporation and lift-off process. In order to reduce the contact resistance of metal-SnS_2 for better device performance, Ti ($W_m = 4.33$ eV) was adopted for realizing n-type contacts and the low Schottky barrier for electrons at the SnS_2/Ti interface due to its low working function. Figure 4(a) shows the optical image of a fabricated SnS_2/Si vertical tunnel diode in this study. The thickness SnS_2 in this tunnel diode is about 50 nm, measured by the atomic force microscope (AFM), as shown in Figure 4(b). The characteristic Raman peaks of SnS_2 can be distinctly observed, as shown in Figure 4(c). The A_1g peak of SnS_2 is observed at 315.0 cm^{-3}.

3 Results and discussion

Figure 5 shows the measured electrical characteristics of the N^+ SnS_2/P^+ Si tunnel diode at room temperature. The results are obtained by applying the bias V_P on Si contact, with SnS_2 contact grounded. Figure 5(a) shows the bidirectional conductivity. The thermionic emission current dominates in the forward bias region, while the Zenner tunneling current dominates in the reverse bias region. The N^+

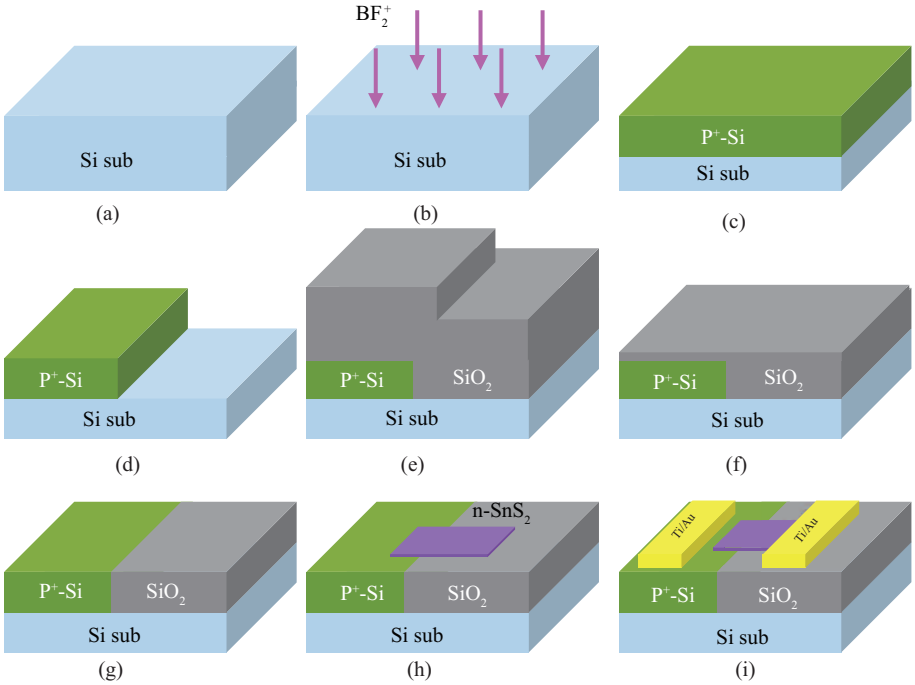

Figure 3 (Color online) The details of the process to fabricate the vertical N^+ SnS_2/P^+ Si tunnel diode. (a) The original Si substrate; (b) ion implantation with $BF_2{}^+$; (c) highly p-doped Si; (d) dry etching to form trenches; (e) CVD of SiO_2; (f) CMP of SiO_2; (g) HF treatment to remove the residual and native oxide; (h) transfer of SnS_2 sheet; (i) formation of contacts.

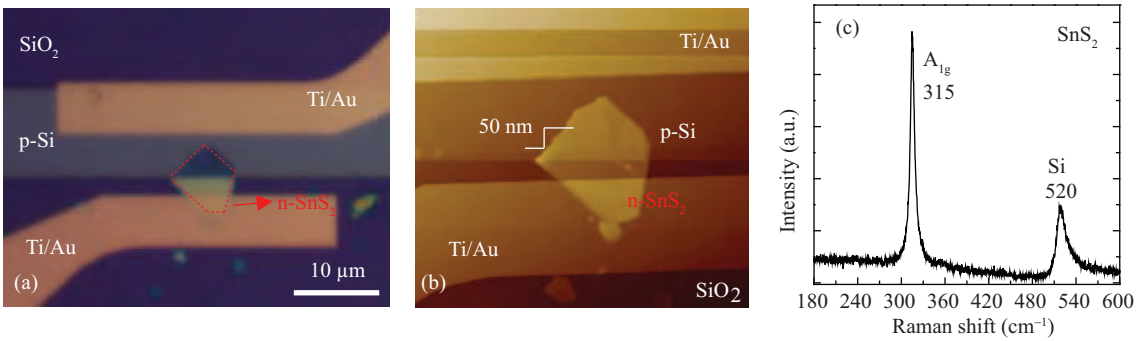

Figure 4 (Color online) (a) The optical microscope image of the fabricated vertical N^+ SnS_2/P^+ Si tunnel diode; (b) AFM image of fabricated vertical N^+ SnS_2/P^+ Si tunnel diode; (c) Raman characterization of the SnS_2 sheet in the tunnel diode.

SnS_2/P^+ Si tunnel diode exhibits high Zenner tunneling current of 12.8 μA and the tunneling current density is 1 $\mu A/\mu m^2$, which is higher than that in the reported N^+ MoS_2/P^+ Ge and N^+ MoS_2/P^+ Si tunnel diodes [2,12], further confirming the optimized band alignment of the N^+ SnS_2/P^+ Si heterostructure. In the N^+ MoS_2/P^+ Ge tunnel diode, the relatively larger effective tunnel barrier height (0.4 eV), together with the native oxide of Ge at the interface which is formed during the fabrication process, limits the current density of the tunneling devices [2]. In the N^+ MoS_2/P^+ Si tunnel diode, although the band diagram changes from type-I to type-II as the thickness of MoS_2 increases from the monolayer to the bulk, the tunnel diode exhibits the unsatisfactory tunneling current due to the large effective tunnel barrier height (0.78 eV) [14]. However, in the N^+ SnS_2/P^+ Si tunnel diode of this study, the effective tunnel barrier height is optimized to be 0.17 eV which is much lower than that in the N^+ MoS_2/P^+ Ge or N^+ MoS_2/P^+ Si tunnel diodes. According to the results in [12,17–19], SnS_2 with thickness of 50 nm is partially depleted. Although the thickness of SnS_2 in this experiment is relatively large, the tunneling current density is still the highest one compared with that of N^+ $MoS_2/$ P^+ Ge and N^+ $MoS_2/$ P^+ Si

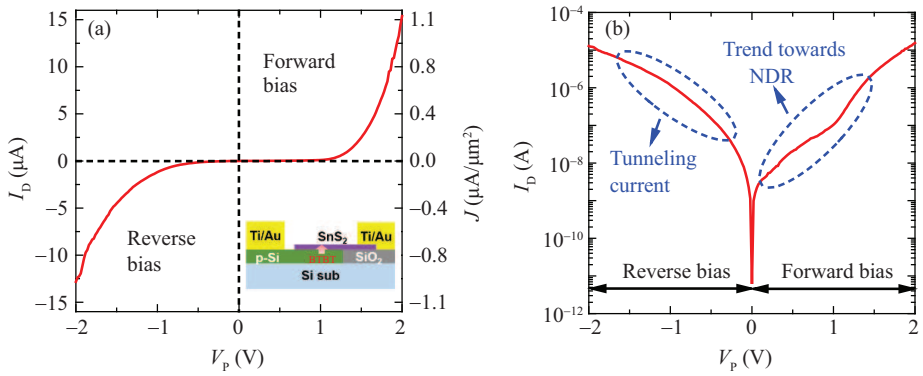

Figure 5 (Color online) The electric characteristics of the vertical N^+ SnS_2/P^+ Si tunnel diode. (a) Linear and (b) log current-voltage characteristics.

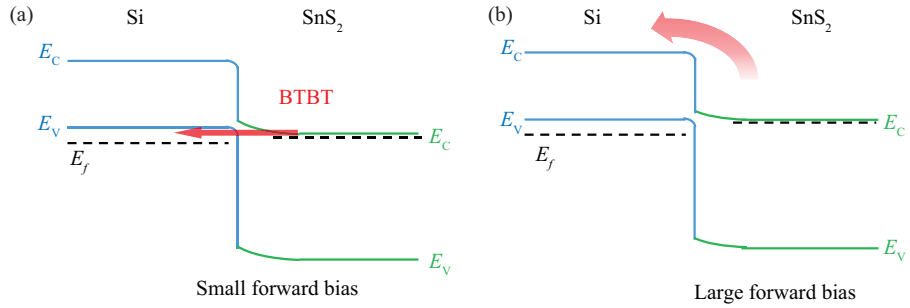

Figure 6 (Color online) The NDR characteristic of the vertical N^+ SnS_2/P^+ Si tunnel diode. (a) The band diagram in the small forward bias region; (b) the band diagram in the large forward bias region.

tunnel diodes. By future decreasing the thickness of SnS_2, the effective tunneling barrier width can be further reduced and the tunneling current will increase considerably. Furthermore, during the fabrication process, the HF treatment of the silicon substrate removes the native oxide, and thus effectively improves the tunneling efficiency and tunneling current.

As shown in Figure 5(b), a trend towards negative differential resistance (NDR) in the forward bias region is observed and confirms that a heavily-doped N^+ SnS_2/P^+ Si junction is formed at the interface. To illustrate this phenomenon, the band alignment of the N^+ SnS_2/P^+ Si tunnel diode under different forward bias conditions is given in Figure 6. In the equilibrium state, the Fermi level in p-type Si and n-type SnS_2 is aligned, as shown in Figure 2(b). As the forward bias V_P increases, the energy band of Si is pulled down, and a finite tunneling window is created for electrons in the conduction band of SnS_2 to tunnel into the empty states in the valence band of Si. The tunneling current reaches its peak when the Fermi level of SnS_2 aligns with the valence band maximum of Si, as shown in Figure 6. As the increase of the forward bias V_P, the tunneling window is gradually switched off, meanwhile, the thermionic current begins to dominate and is larger than the tunneling current, leading to the transition from tunneling to thermionic emission and showing a trend towards NDR.

In order to further verify the tunneling mechanism of this vertical N^+ SnS_2/P^+ Si tunnel diode, the dependence of electric characteristics on temperature is studied. Temperature dependence of thermionic current in forward bias and tunneling current in reverse bias region are compared in Figure 7. Both mechanisms of current show positive dependence on temperature. With the decreased temperature, the bandgaps of silicon and SnS_2 relatively increase, which has been experimentally observed in [20,21]. The increased bandgaps will lead to the decreased tunneling probability and decreased current for tunnel diode. For thermionic emission current, the fermi distribution also changes with temperature, and the number of electrons with high energy decreases at low temperature, resulting in the lower thermionic emission current. However, the correlation coefficients of these two kinds of current are different. Tunneling current shows the weaker dependence on temperature than the temperature dependence of the thermionic

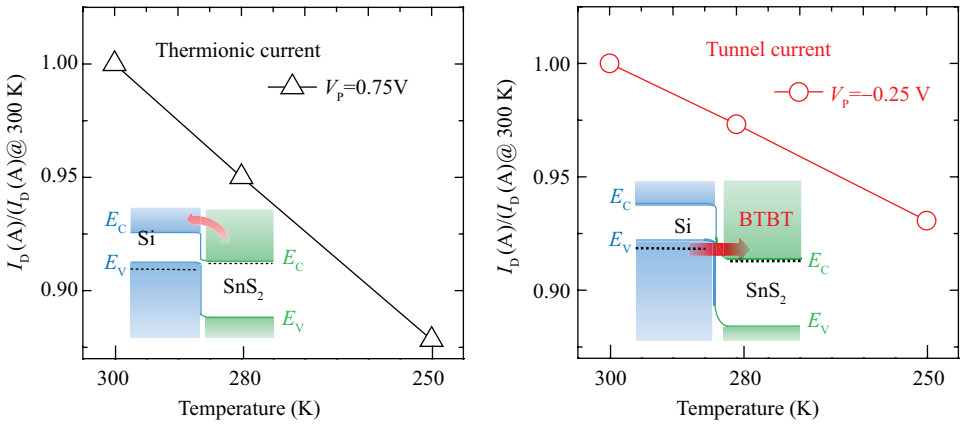

Figure 7 (Color online) The temperature characteristic of the vertical N^+ SnS_2/P^+ Si tunnel diode.

emission current in the forward bias region, which is the typical feature of tunneling current [22]. This is due to the different sensitivity of the bandgap and the Fermi distribution. Since the bandgap shows the weaker dependence than the Fermi distribution on the temperature, the tunneling current shows the weaker dependence as shown in Figure 7.

4 Conclusion

In conclusion, the N^+ SnS_2/P^+ Si heterostructure with effective tunnel barrier height of 0.17 eV theoretically is considered for the first time and the vertical tunnel diode is experimentally demonstrated to verify the superiority of the N^+ SnS_2/P^+ Si heterostructure. This fabricated N^+ SnS_2/P^+ Si tunnel diode shows the high current density of 1 $\mu A/\mu m^2$, which is the highest one among the reported tunnel diodes based on the 2D/group IV materials. The tunneling current is also confirmed by the low-temperature measurements. This study shows the great potential of the 2D/3D heterostructure for low-power tunneling devices.

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