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Low power and high uniformity of HfO_x-based RRAM via tip-enhanced electric fields

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Abstract In this paper, the HfO_x-based resistive random access memory (RRAM) devices with sub-100 nm pyramid-type electrodes were fabricated. With the help of tip-enhanced electric field around the pyramid-type electrodes, it was experimentally demonstrated that the novel devices have better cycle-to-cycle variation control, lower forming/set voltage (1.97/0.7 V) and faster switching speed ($\leqslant$ 30 ns under 0.9 V pulse) as well as better endurance reliability than conventional flat electrode resistive memory devices. In addition, the novel RRAM is experimentally demonstrated with independence of electrode number for the first time to present great potential in scaling down. This novel structure metal-oxide based RRAM will be suitable for the future low-power non-volatile memory application.

Keywords RRAM, pyramid-type electrode, variation, reliability, switching speed, conducting filament

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1 Introduction

Metal-oxide resistive random access memory (RRAM) has been extensively studied and considered as the next generation nonvolatile memory device due to its fab-friendly feature, fast switching speed and low energy consumption [1–4], especially for embedded application. Meanwhile, many researches have been conducted to reveal the conductive mechanism [3–5]. The most compelling physical model is the "conducting filament model", which has been demonstrated by many researchers [6–8]. This model explains the resistive switching by the formation and rupture of conductive filaments (CFs) in the metal-oxide zone. However, there is some randomness during the growth and dissolution of CFs, leading to large operation voltage variation and non-negligible resistance dispersion [9]. At the meantime, an effective way to further reduce switching voltage is critical to the low power application. Various methods have been developed to improve switching uniformity and energy efficiency. For example, ion-doped RRAM was reported to have high uniformity of switching parameters [10] and low operation voltages [11, 12]. Bilayer or tri-layer resistive switching structures were used to reduce switching variation and operating currents [13, 14]. In addition, the electrode engineering is also very effective in realizing low-power performance with promising uniformity. For instance, conducting bridge RAM (CBRAM) with low set/reset voltages and improved resistance uniformity was realized by micron-scale pyramid-electrode structure [15, 16], which greatly increases the electric field intensity around the tip. However, the impact

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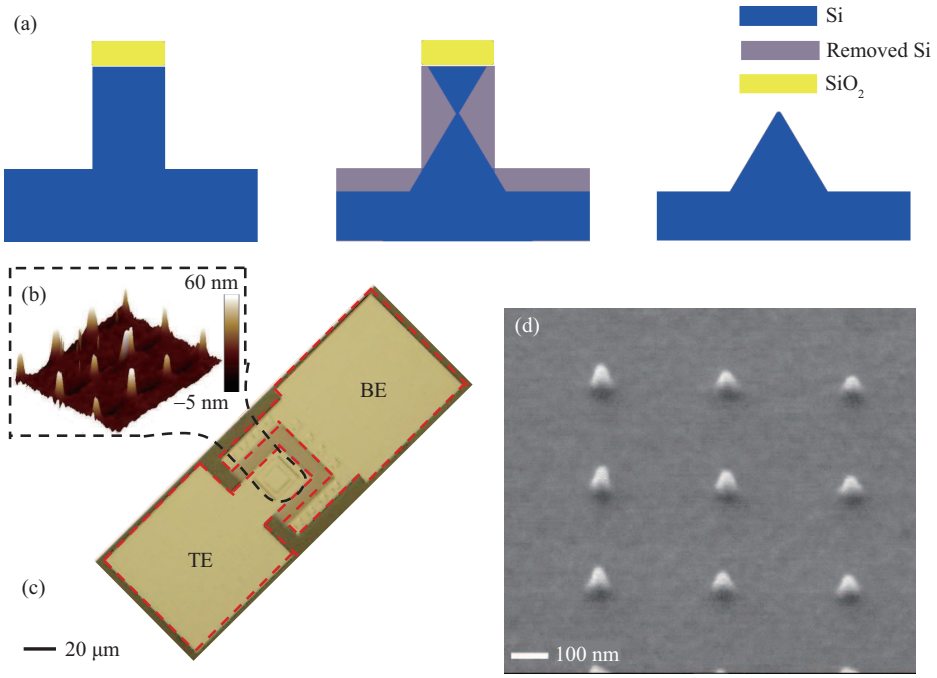

Figure 1 (Color online) (a) Schematic diagrams of main flow to fabricate Si-pyramid; (b) AFM image of the pyramid structure; (c) the optical microscopy photograph of the fabricated Pt/HfO_x/Ti/Al RRAM; (d) SEM image of the Si-pyramid.

of nanometer-scale modified electrode with tip-enhanced electric field on oxygen-vacancy-based RRAMs have been not studied.

In this paper, we fabricated the Pt/HfO_x/Ti/Al RRAM devices (12 μm×12 μm) with sub-100 nm pyramid-type electrodes and investigated the impacts of tip-enhanced electric field on oxide-based RRAM for the first time. Results show that low operation power and high cycle-to-cycle uniformity of oxide-based RRAM can be achieved by the novel structure. The physical mechanism inside the enhanced conductive switching operation was also discussed in depth.

2 Experiment

Figure 1(a) shows the main flow of fabricating pyramids on Si substrate. Firstly, the Si quadrangular prisms were patterned by e-beam lithography and followed by reactive ion etching on p-type (100) oriented crystalline wafer. Then, two continuous process steps were carried out to remove the native oxide with hydrofluoric acid firstly and then form the pyramid structures with 25 wt% Tetramethylammonium Hydroxide (TMAH). A 40-nm thick Pt layer was deposited by magnetron sputtering system to act as the bottom electrode. Subsequently, a 5-nm-thick HfO_x layer was deposited by atomic layer deposition (ALD) as switching oxide layer. Finally, 40-nm thick Ti and 40-nm thick Al layers were deposited as the oxygen-gettering layer and the top electrode, respectively. The conventional flat electrode RRAM were also fabricated as the control group. The optical microscopy photograph of the fabricated pyramid-type RRAM is shown in Figure 1(c). Atomic force microscope (AFM) image and scanning electron microscope (SEM) image of the pyramid structure are shown in Figure 1(b) and (d), respectively. From AFM and SEM results, the height and the side length of pyramid is measured to be about 65 and 70 nm, respectively. The electrical characterizations of the device were then carried out with Agilent B1500A analyzer.

3 Results and discussion

For simplicity, PE and FE are referred to pyramid-type electrode memory and conventional flat-type electrode memory, respectively. The current compliance (I_{comp}) is set to 500 μA to avoid breakdown.

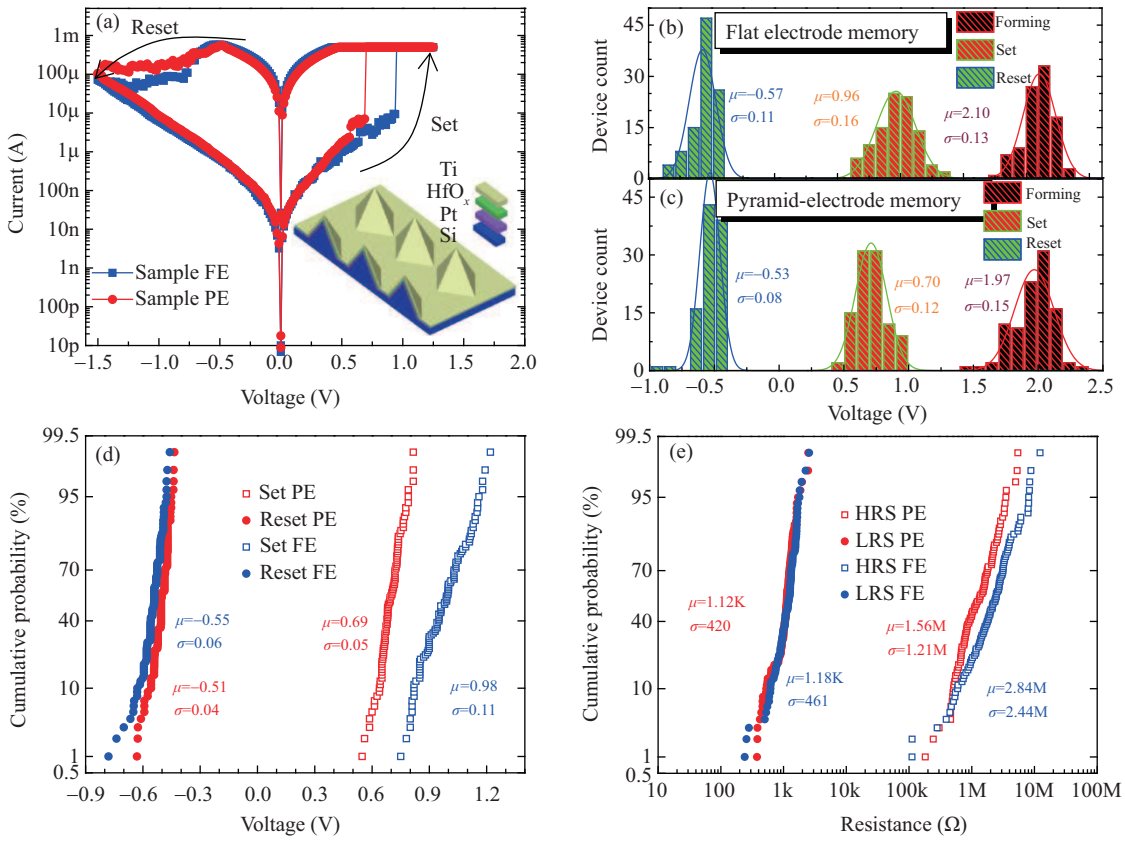

Figure 2 (Color online) (a) The typical DC sweep curves of PE and FE. The uniformity of the switching voltages obtained by DC sweep operation for 100 devices of (b) FE and (c) PE. The cumulative probability of (d) set/reset voltages and (e) HRS/LRS for 100 continuous DC sweep cycles.

Figure 2(a) shows the typical resistive switching curves of the two samples under direct current (DC) sweep operation. By testing 100 devices for each type and extracting the feature switching voltages shown in Figure 2(b) and (c), it can be clearly seen that both forming voltage and set voltage of PE are lower than FE, but reset voltages of two samples do not show much difference. Except forming voltage, both set voltage and reset voltage distribution are narrower for PE than for FE. Furthermore, the cumulative distribution of switching voltage during 100 continuous DC sweep cycles are plotted in Figure 2(d) to measure the cycle-to-cycle variation. From the plotting, PE shows lower and more tightly distributed set voltage than FE. Figure 2(e) shows the resistance distribution at high resistance state (HRS) and low resistance state (LRS). The results show that the two types of devices have the similar median and deviation of LRS, but the PE has lower and tighter distribution of HRS than FE. From the comparison, pyramid-type RRAM has shown better device-to-device uniformity and less cycle-to-cycle variation.

On the other hand, the impact of tip-enhanced field on memory reliability was also investigated. In Figure 3(a), (c) and (d), the endurance and retention characterization are compared for two samples. During the endurance stress, the set and reset pulses are set to be (1.4 V, 22.5 ns) and (−1.5 V, 100 ns), respectively. The testing method used in Figure 3(a) is collecting 10 points per decade during pulses stresses, the endurance characterized by this mode is fast and the experimental spaced data can be clearly distinguished. However, it cannot display the complete millions of switching transitions. Extracting HRS and LRS for each cycle by current-visible pulsed voltage stresses (PVS) method in [17] is recommended. In Figure 3(b), we only test and show data from the first 5000 cycles of PE because of lacking rapid measurement hardware and limited testing time. Considering the stable switching with 100 times resistance ratio in Figure 3(b) and spaced points obtained by current-blind PVS tests in Figure 3(a), it is expected that about 10^7 set/reset switching cycles of PE can be achieved, in the other hand, only 10^6 cycles can be repeated for FE, as seen from Figure 3(a). Although, this result is still not good as the

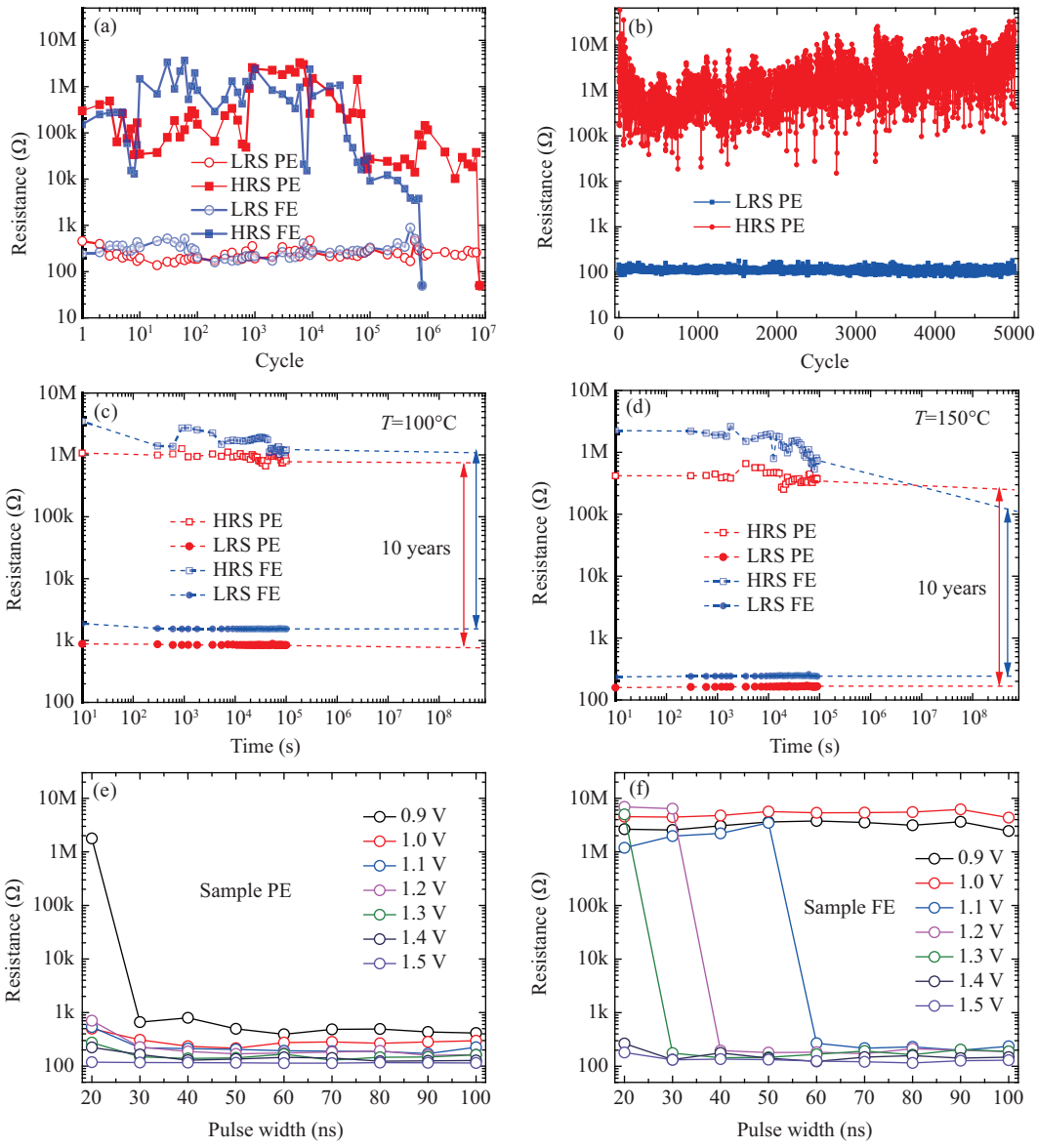

Figure 3 (Color online) (a) Switching endurance of PE and FE under the set pulse (1.4 V, 22.5 ns) and reset pulse (−1.5 V, 100 ns) without verification. (b) The resistance transitions of PE for each cycle under the same pulse conditions in (a). The data retention of PE and FE at (c) 100°C and (d) 150°C. The resistance after set by varied pulsewidths under gradual increasing pulse amplitude in (e) PE and (f) FE.

record, it can be further improved by adopting the current limiter, such as the 1T1R configuration to raise up the LRS to suppress the joule heat buildup and then improve the endurance performance [18]. For the reasons of improved endurance in PE, it may be attributed to the reduced randomness of filaments in position and shape, which can induce higher uniformity of switching parameters and thus reduce the failure probability to improve endurance characteristics. Furthermore, both LRS and HRS of PE and FE can keep 1000 times resistance ratio for 10 years under 100°C baking condition as shown in Figure 3(c). However, PE shows less HRS instability than FE to indicate better "0" state retention capability. Additionally, in Figure 3(d), compared with PE, significant resistance degradation appeared in FE when the temperature was increased to 150°C, which suggests that higher temperature can facilitate atomic rearrangements and PE may have better thermal dissipation capability, The related self-heat problem of PE will be studied in our future work. Nevertheless, from the above comparisons, it can be seen that the tip-enhanced field does "improve" rather than degrade the memory reliability of oxide-based RRAM.

For low-power application, a fast switching operation would be an extra advantage. In order to

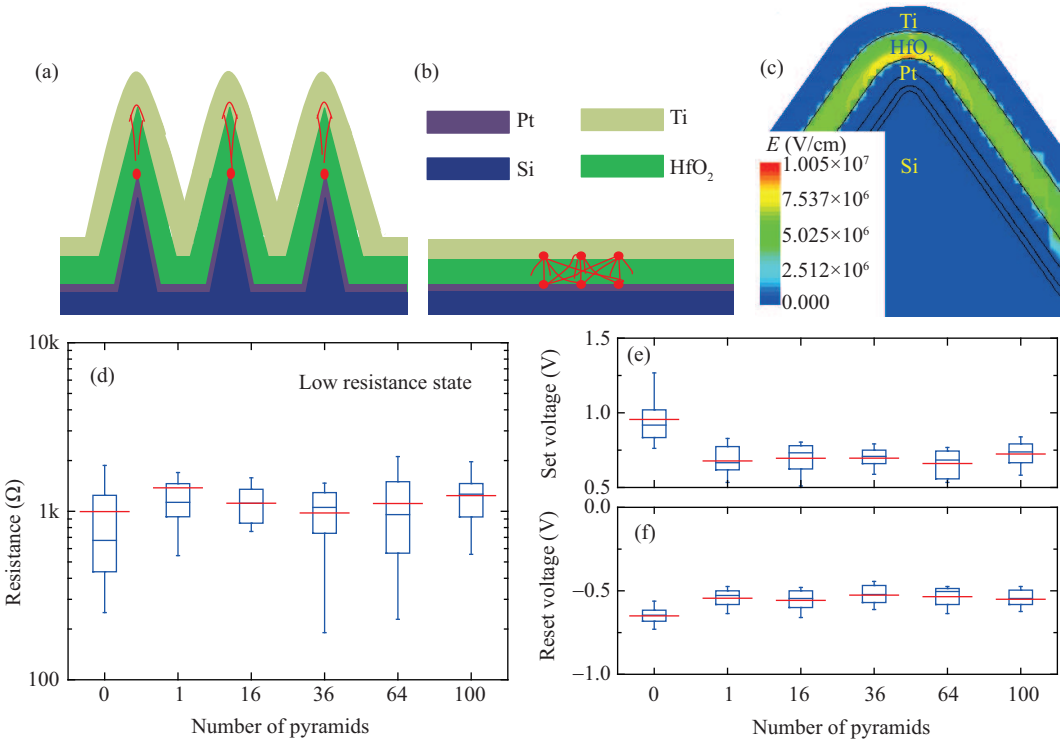

Figure 4 (Color online) Comparative illustrations of the morphology of the CFs in the (a) PE and (b) FE. (c) The electric field of the tip area simulated by Synopsys TCAD Sentaurus tools. The influence of number of pyramids on the (d) LRS, (e) set volatge and (f) reset voltage of 20 cells.

investigate the impact of tip-enhanced electric field on the switching speed of oxide-based RRAM, the set operations were carried for different durations for both samples. For each set operation, PE and FE were initially reset to HRS by applying a long reset pulse under −1.5 V with 100 ns. Then, two samples were set from HRS to LRS with various set pulse-widths and voltage amplitudes. To avoid the impact of read voltage on the results, the resistance sampling was carried out by a short pulse with very small amplitude of 30 mV and width of 100 μs. As seen from Figure 3(c) and (d), even with the set pulse amplitude as low as 0.9 V, PE can still be successfully set to LRS within 30 ns. As for FE, however, the pulse-width for effective programming approximately equals to 60 ns even when the pulse amplitude is 1.1 V. It means that PE can achieve faster set operation under lower operation voltage than FE. It indicates that the tip enhanced field would be more advantageous for low power application than the uniform field in the flat electrode.

To better understand the mechanism behind the improved switching characteristics of pyramid-type RRAM, the 3D simulation of electric field is carried with Synopsys TCAD Sentaurus. In the simulation setup, the radius of curvature of the Pt pyramid electrode is set to 2 nm, which is deduce from the statistical results in AFM and SEM images. The cross-sectional electric filed profile along the direction from top tip to bottom substrate is shown in Figure 4(c). The electric filed intensity around the tip is about 3 times of that on the flat surface, which is beneficial to generate or dissolve the oxygen vacancies. According to (1) [9, 19],

$$P = (t/t_0)\exp[-(E_a - b|E|)/kT],$$

where $1/t_0$ is the characteristic vibration frequency of oxygen vacancy, E_a is the height of migration barrier, E is the local electric field, b is the bond polarization factor, and the local enhancement factor b/kT equals about 3 [9]. The oxygen vacancy generation possibility (P) is enhanced by about 52 times with pyramid-type RRAM relative to flat-type RRAM. As a result, the forming voltages of pyramid-type RRAM are lower than those of flat-type RRAM. Moreover, the residual Vo filament tip after reset is retained in the region with higher electric fields, and the enhanced electric field can activate more

oxygen vacancies and induce faster migration along the electric field lines, which is sort of benefit for the assembling of oxygen vacancies near the filament tip during set operations, so the field enhancement effect can lead to lower a set voltage in PE. In addition, there is high concentration of oxygen vacancies near the top Ti/HfO_x interface due to the oxygen-gettering effect. So it is expected that the filament will dissolve and reconnect in the middle part, which is the weakest point of the filament. However, it is just a speculative physical image which needs more scientific data to support. And the in-situ observation of Vo filaments can help to reveal the mechanism, which may be realied in the future.

On the other hand, the electrons hopping frequency between two vacancies will significantly enhanced by the increased tip electric field according to Mott model [20, 21],

$$R_{nm} = R_0 \exp[r_{nm}(qE_{nm}/kT - 1/a_0)],$$

where R_0 is vibration frequency of electrons, r_{nm} is the distance between the two vacancies, a_0 is the relaxation length of the electron wave function, E_{nm} is the local electric field between the two vacancies caused by external electric field. Assuming that r_{nm} equals to 0.45 nm [22], the hopping rate will be significantly increased from 7.7×10^{13} to 8.9×10^{18} Hz by pyramid-type electrode. The hopping conductance is thus enhanced and lower set resistance is obtained even at the same set compliance limit.

Moreover, the tip-enhanced field also helps to improve the HRS endurance stability and high-temperature retention due to more complete dissolution of CFs during reset operation than that in flat-type RRAM.

For uniformity and reliability consideration, the configurations of CFs at LRS are schematically depicted in Figure 4(a) and (b) for pyramid-type and flat-type, respectively. Usually, the formation and distribution of nanoscale CFs in the flat type RRAM is quite random and triggered by the surface roughness and defects [23,24]. Once a CF forms, the selective low resistive path will make the current crowding so that the formation of other CFs will be suppressed and stay incomplete. If there is no CF seeds, i.e., defects in the area, the forming or set operation will become difficult and mainly depend on the oxygen diffusion rate in the oxide layer. Therefore, conventional flat-electrode RRAM will show area-dependent resistance as the area is scaled down to 0.01 μm^2 [25, 26]. The switching voltages are even more dependent on the area [25]. It will put an area limitation on RRAM for large density integration. In pyramid-electrode RRAM, however, such CF formation process will be enhanced no matter there are defects or not. It makes the formation of CFs easier and more localized around the tip to improve the uniformity and reduce the operation voltage. As an important result, the resistance and operation voltages will keep constant with different number of pyramids, as shown in Figure 4(d), (e) and (f), since the number of pyramids does not affect the peak electric field. Such independence of set/reset operation on pyramid number will help oxide-based RRAM to scale down.

4 Conclusion

In conclusion, a novel HfO_x-based RRAM with sub-100 nm pyramid-type electrodes was proposed and fabricated on Si substrate. Thanks to the improved localization of CF formation by tip-enhanced field, the pyramid-type RRAM shows low operation voltages, high uniformity and fast switching speed compared to conventional flat-type RRAM. The pyramid-type RRAM will be potential in future scaled low-power high-density memory application.

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