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Deep insight into the voltage amplification effect from ferroelectric negative capacitance

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Dear editor,

Power dissipation has become one of the most serious problems for nano-electronics. For conventional transistors, the operation voltage cannot be continuously reduced due to the fundamental limitation of subthreshold swing (SS) (60 mV/decade at room temperature) [1, 2]. The voltage amplification (VA) induced by the negative capacitance (NC) effect of ferroelectric (FE) material provides a possible approach for FE-based transistors to achieve sub-60 SS characteristics [3]. However, the physical origin of NC effect in FE-FET are still unclear and controversial. The traditional quasi-static NC theory considers that the NC can be derived from the negative curvature of energy-charge relationship of ferroelectric, which is unstable for standalone FE capacitor and can be stabilized by connecting an appropriate positive capacitor to reach a capacitance matching condition for VA [3]. Different with quasi-static NC theory, it has been recently presented that the NC effect can be modeled as a transient phenomenon caused by the FE polarization switching [4, 5]. In [5], we have demonstrated the first direct experimental observation of NC phenomenon in a standalone FE capacitor, verifying its dynamic behavior. It is shown that the time-induced polarization is the origin of NC phenomenon. Nevertheless, further study on the optimization of gate stack in FE-FETs for achieving VA is still needed.

In this study, based on [5], we provide more detailed insights into the dynamic behavior of NC for the VA of FE-FET and present a comprehensive study on the condition of VA. First, the experimental observation of VA in the gate stack structure is presented, showing its dynamic behavior. Then, the specific condition of VA is studied taking the ferroelectric dynamic behavior into consideration. A dynamic polarization matching condition is presented and discussed in detail. At last, the simulation based on ferroelectric polarization dynamics is performed to enlarge the VA effect in terms of voltage sweeping rate, ferroelectric parameters and series capacitance.

We demonstrate experimental verification on mechanism of VA effect in gate stack structure, showing its dynamic behavior. Then based on it, VA effect with ferroelectric dynamic behavior into consideration is studied. As a result, dynamic polarization matching condition is proposed for VA effect realization. Simulation based on ferroelectric polarization dynamics is then established to study VA effect optimization in terms of voltage sweeping rate, ferroelectric property and series capacitance.

Experiment and measurement. In FE-FET, the FE capacitance is not isolated in the gate stack. To investigate the VA effect in FE-FETs, we fabricated a capacitor series system consisted of an FE capacitor and a positive dielectric capacitor to characterize the device gate stack. In this study, we chose Zr-doped HfO_2 as the FE material, due to its excellent compatibility with CMOS process [6]. As shown in Figure 1(a), to fabricate the capacitor

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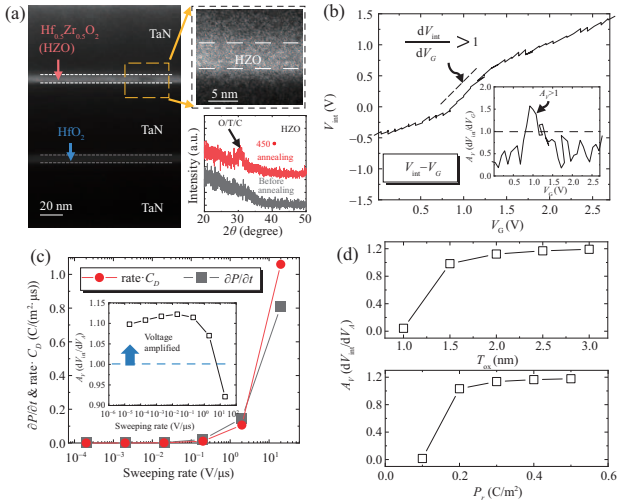

Figure 1 (Color online) (a) TEM image of capacitor series structure in this work and XRD of $HfZrO_2$; (b) measured $V_{\rm int}$ versus V_G in the capacitor series structure; (c) different dynamic polarization matching situations and corresponding A_V (inset) for different sweeping rate; (d) A_V for different thickness of oxide $T_{\rm ox}$ and remanent polarization P_r.

series system, metal layer of TaN, dielectric layer of HfO_2 and TaN layer are deposited on silicon substrate in turn. Next, the Zr-doped HfO_2 (HZO) was obtained by atomic layer deposition with an Hf:Zr ratio of 0.5:0.5 consisting of one cycle of HfO_2 and one cycle of ZrO_2. The thickness of HZO is about 5 nm. Then, the top electrode of TaN layer was sequentially deposited. The annealing process was performed in an N_2 environment under 450°C to crystallize the HZO film and activate its ferroelectricity. The transmission electron microscope (TEM) image and X-rays diffraction (XRD) in Figure 1(a) further confirm its polycrystalline nature and the formation of non-centrosymmetric ferroelectric phase [7].

To investigate the VA behavior of FE in this capacitor series system, a sweeping gate voltage (V_G) with a constant sweeping rate on this total series system is applied, and the voltage across the internal positive capacitor ($V_{\rm int}$) is measured. The amplification coefficient (A_V) can be extracted from the slope of $V_{\rm int} - V_G$ curves, which indicates the differential change of $V_{\rm int}$ modulated by V_G. As shown in the extracted $A_V - V_G$ curve of Figure 1(b), it can be seen that the A_V can exceed 1 or the VA can be obtained within a specific range of gate voltage. In addition, standalone FE capacitor is connected to the ferroelectric test system (radiant premier II), and the monitored voltage across FE capacitor ($V_{\rm FE}$) in FE-DE gate stack is programed as input voltage. Then the negative slope polarization-voltage curve is observed directly. Moreover, the VA or NC effect can only occur over a narrow frequency range of sweeping voltage [5]. It indicates that the internal voltage can be amplified only under some certain conditions.

Condition for VA effect. Based on the above discussion, the condition for obtaining VA in the gate stack structure can be derived as follows. The ferroelectric polarization switching is a time-dependent process with the domain nucleation growth predominated. Hence, the FE polarization (P) increment includes the ferroelectric voltage (V_F) induced increment and the time (t) induced increment:

$$\mathrm{d}P = (\partial P/\partial V_F)\cdot \mathrm{d}V_F + (\partial P/\partial t)\cdot \mathrm{d}t. \quad (1)$$

Besides, according to the charge balance equation, the P of FE in the series system, consisting of both ferroelectric and paraelectric parts, equals to the charge (Q) of dielectric capacitor (C_D). Thus, the differential increment of $V_{\rm int}$ can be written as: $\mathrm{d}V_{\rm int} = \mathrm{d}P/C_D$. By combining it, (1), and the voltage dividing relationship ($\mathrm{d}V_F = \mathrm{d}V_G - \mathrm{d}V_{\rm int}$), the A_V can be derived as follows:

$$A_V = \frac{\mathrm{d}V_{\rm int}}{\mathrm{d}V_G} = \frac{1}{C_D}\left[\frac{\partial P}{\partial V_F}\left(1 - \frac{\mathrm{d}V_{\rm int}}{\mathrm{d}V_G}\right) + \frac{\partial P}{\partial t}\frac{\mathrm{d}t}{\mathrm{d}V_G}\right]. \quad (2)$$

Therefore, according to (2), the A_V ($\mathrm{d}V_{\rm int}/\mathrm{d}V_G$) can be simplified:

$$A_V = \left(\frac{\partial P}{\partial V_F} + \frac{\partial P}{\partial t}\frac{\mathrm{d}t}{\mathrm{d}V_G}\right) \Big/ \left(\frac{\partial P}{\partial V_F} + C_D\right). \quad (3)$$

According to (3), to obtain the voltage amplification, the below condition should be satisfied:

$$\partial P/\partial t > \mathrm{rate}\cdot C_D \quad (\mathrm{rate} = \mathrm{d}V_G/\mathrm{d}t). \quad (4)$$

The above formula gives the prerequisite matching condition for VA effect in gate stack of FE-FET. Since it is derived based on FE dynamic polarization physics, this condition is called dynamic polarization (DP) matching. Different from

the quasi-static capacitance matching condition, this dynamic condition indicates that the A_V can be larger than 1 only when the FE polarization switching speed ($\partial P/\partial t$), under certain input voltage is larger than the charge increment rate of CD in response to the input voltage ($\mathrm{d}V_G/\mathrm{d}t \cdot C_D$).

Dynamic simulation. Based on the above discussion, the time involved simulation of FE-FET is further carried out. The FE dynamics can be described successfully by the classic Kolmogorov-Avrami-Ishibashi (KAI) model [8], which can be expressed as: $P_{\mathrm{fe}} = P_r(1 - \exp(-t/t_s))$. The P_r is the spontaneous polarization of FE. The t_s is the switching time, which is defined as the time of current reaching the maximum in current-voltage transient measurement of ferroelectric, and is related to both material and measurement condition. The t_s varies from nanoseconds to seconds for different materials, and is the most crucial FE parameter when analyzing the dynamic polarization switching behavior of ferroelectric. According to the Merz's Law [9], the t_s can be expressed as a function of time t and electric field E ($t_s = t_s \exp(\alpha/E)$), where t_∞ is the switching time for infinite E and α is a constant obtained from experimental data. By self-consistently coupling the calibrated ferroelectric dynamic polarization with charge balance relationship, the voltage amplification condition of FE-DE series capacitor system can be analyzed.

Considering the dynamic behavior of FE, the influence of voltage sweeping rate on VA is studied. Figure 1(c) shows the simulated dynamic polarization matching situations for various V_G sweeping rates. As sweeping rate increases, rate $\cdot\, C_D$ finally become larger than $\partial P/\partial t$ when the rate is larger than 6 V/us, which indicates that the dynamic polarization matching condition is not satisfied at this time and correspondingly A_V will be smaller than 1. Moreover, it should be noted that the $\partial P/\partial t$ would also decrease as the sweeping rate decreasing, even when the dynamic polarization matching condition is satisfied. Inset of Figure 1(c) show the extracted A_V versus V_G for different sweeping rates. It is shown that when the sweeping rate is larger than 6 V/us, the internal voltage cannot be amplified. With reduced sweeping rate, voltage amplification can be obtained with $A_V > 1$, while the A_V will slightly decrease at relatively slow sweeping rate due to the reduction of $\partial P/\partial t$.

Besides the sweeping rate, the proposed dynamic polarization matching condition indicates that the VA of FE is related to the FE polarization switching speed ($\partial P/\partial t$) and the series dielectric capacitance (C_D). From KAI formula, the polarization switching speed can be derived as follows: $\partial P/\partial t = P_r(1+t_s^{-1}\cdot\exp(-t/t_s))$, which is related to spontaneous polarization P_r. As for C_D, it is directly related to the dielectric thickness, permittivity and area. As shown in Figure 1(d), the dynamic polarization matching situations and A_V $-V_G$ curves with various P_r and C_D are also simulated (Figure 1(d)), showing that the larger P_r and the thicker dielectric layer would result in the faster polarization switching and the smaller C_D, leading to the larger voltage amplification effect.

In conclusion, we have presented the direct observation of voltage amplification in ferroelectric HZO based gate stack structure, verifying its dynamic behavior. A dynamic polarization matching condition for VA of FE is further proposed. Based on the experimental data and the derived matching condition, the VA is simulated and extracted under different voltage sweeping rates, ferroelectric parameters and series capacitances. The results of this study suggest that the faster FE switching and the smaller series capacitance can enhance the VA effect and further SS optimization for FE-FETs.

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