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Physical mechanism of performance adjustment in selective buried oxide n-MOSFETs

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Dear editor,

FDSOI MOSFETs do not rely on channel doping to control short channel effects; they overcome the barriers of conventional bulk MOSFETs by means of scaling. Owing to the presence of the buried oxide insulator (BOX), FDSOI MOSFETs offer many additional benefits over bulk MOSFETs. Some important advantages being: (i) total dielectric isolation to reduce junction leakage, capacitance, and latch-up immunity; (ii) ultra-thin buried oxide (BOX) and back-plane (BP) doping to enable back-biasing for the threshold voltage (V_t) tunning [1,2]. However, the self-heating effect (SHE) poses a challenge to the use of FDSOI MOSFETs. With a decrease in device size, nanometer-scale hot spots are created in the transistor drain region [3], and this problem is worse in the case of FDSOI MOSFETs. Because its thermal conductivity (1.4 W/m·K) is much lower than that of bulk silicon (148 W/m·K) [4], the BOX impedes heat conduction. Moreover, the thermal conductivity of the active device region, i.e., the thin-film body silicon on insulator (SOI), is much lower, because it is directly proportional to the film thickness [4]. The selective buried oxide (SELBOX) MOSFETs has a window in the BOX under the channel and efficiently mitigates the problem of SHE [5,6]. In the previous studies, the BOX window was located under the center of the channel, although the hot spots were located near the drain region. This study deals with the influence of the position of the BOX window on the thermal and direct current (DC) performance in n-type SELBOX MOSFETs with n-type BP doping. Peak lattice temperature and DC performance were investigated via two-dimensional simulations, and the underlying physical mechanisms were analyzed in detail via comparison with FDSOI MOSFETs.

Device structure. The basic structures of the SELBOX and FDSOI MOSFETs are illustrated in Figure 1(a). The BOX window region in SELBOX MOSFETs and the back bias region in FDSOI MOSFETs can be synchronously implemented by trench etching and silicon epitaxial growth. The X direction points to the drain side, and the center of channel is located at $X_0 = 0$. The center of BOX window $X_{\rm gap}$ represents the position of the window, and $L_{\rm gap}$ represents the size of the window. The simulated devices have an effective channel length of 25 nm, a 6 nm SOI film with a p-type doping level of 1×10^{15} cm^{-3}, a BOX of 20 nm, and a same n-type BP doping profile as that in [2].

Device operations. The thermal and DC performance (with SHE) of SELBOX MOSFETs with different BOX window locations and FDSOI MOSFETs with different back bias voltages were simulated, as illustrated in Figure 1(b). SELBOX

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MOSFETs with fixed size and different locations have different thermal and DC performance. As the hot spots approach the drain region, the BOX window located under the hot spots exhibits the highest heat dissipation efficiency, leading to the lowest peak lattice temperature, as illustrated in Figure 1(b). With regard to the DC performance, the saturation current shows a rising trend as the BOX window shifts from the source to drain side, except when the BOX window is partially located under source ($X_{\rm gap} = -15$ nm). With regard to FDSOI MOSFETs, the saturation current and peak lattice temperature rise simultaneously as the back bias voltage increases. When the BOX window is located under the source side ($X_{\rm gap} = -26$ nm), SELBOX MOSFETs have the same peak lattice temperature and saturation current as FDSOI MOSFETs with a zero back bias. When the BOX window is located under the drain side ($X_{\rm gap} = 26$ nm), SELBOX MOSFETs have lower lattice temperature and higher saturation current than FDSOI MOSFETs with a back bias of 0.9 V. In addition, regardless of SHE, the changed trend of saturation current remains the same, and the saturation current of SELBOX MOSFETs with the window located under the drain side is equal to that of FDSOI MOSFETs with a back bias of 0.9 V.

The effect of the location of the BOX window on the DC performance of SELBOX MOSFETs was explored. For n-MOSFETs, the positive gate bias voltage leads directly to the downward band on the semiconductor's surface, and the Fermi level on the surface is higher than mid-gap. Electron density on the surface is higher than hole density, forming a conductive path between the source and drain, and there is a current if a bias is applied between the source and drain. However, in FDSOI MOSFETs, the threshold voltage, which is closely related to drain current, also depends on the electrostatic potential on the bottom surface [2]. In fact, the BOX window also affects the electrical performance of SELBOX MOSFETs by modifying the electrostatic potential on the bottom surface. Figure 1(c) shows the electrostatic potential distributions on the top and bottom surfaces when the devices work in the saturation state ($V_{\rm gs} = 0.9$ V, $V_{\rm ds} = 0.9$ V). There is no difference between the electrostatic potential on the top surfaces of different devices, but difference exists on the bottom surfaces. In FDSOI MOSFETs, the higher the back bias voltage, the higher are the electrostatic potential on the bottom surface and the current. Compared with FDSOI MOSFETs with a zero back bias, the electrostatic potential on the bottom surface in SELBOX MOSFETs remains constant with the former on the right of the BOX window, decreases near the window, and increases on the left of the window. The smaller the distance between the BOX window and drain side, the higher is the electrostatic potential of the bottom surface on the left of BOX window. If the effect of the decrease is smaller than the increment, the DC performance is enhanced; else, the DC performance deteriorates, as indicated by the point $X_{\rm gap} = -15$ nm in Figure 1(b). Figure 1(d) shows the electrostatic potential distributions of SELBOX MOSFETs with the BOX window out of the channel and FDSOI MOSFETs to compare the difference between the saturation and linear states ($V_{\rm gs} = 0.9$ V, $V_{\rm ds} = 0.05$ V). When the BOX window is located under the drain side, there exists differences between SELBOX MOSFETs and FDSOI MOSFETs with a back bias of 0.9 V only in the linear state. In the linear state, the electrostatic potential of the bottom surface of SELBOX MOSFETs is lower than that of FDSOI MOSFETs with a back bias of 0.9 V. This means that the electrostatic potential of the bottom surface in SELBOX MOSFETs is directly related to drain voltage; the lower the drain voltage, the lower is the electrostatic potential of the bottom surface. The BOX window offers a window path for the voltage from the drain; herein the obtained voltage works as back bias, increasing the electrostatic potential of the bottom surface. Consequently, when the open window is located under the source side, the obtained voltage is equal to that of the source, and SELBOX MOSFETs has the same electrostatic potential as the FDSOI MOSDETs with a zero back bias, as illustrated in Figure 1(d).

Conclusion. Thermal and DC performance dependence of the position of BOX window in SELBOX MOSFETs are explored. Simulation results show that the thermal performance is directly related to the distance between the window and hot spots; a smaller distance leads to a lower lattice peak temperature. Comparison of the electrostatic potential on the channel surfaces reveals the underlying physical mechanism of the dependence of DC performance on the location of the BOX window. The window offers a path for the voltage from the drain, and the obtained voltage works as a back bias, increasing the electrostatic potential on the bottom surface herein. The increment is related to the distance between the window and drain side. The closer the window is to the drain side, the higher are the bottom electrostatic potential and current. In particular, the SELBOX MOSFETs with a BOX window near the drain side, where the left ends of the window and gate

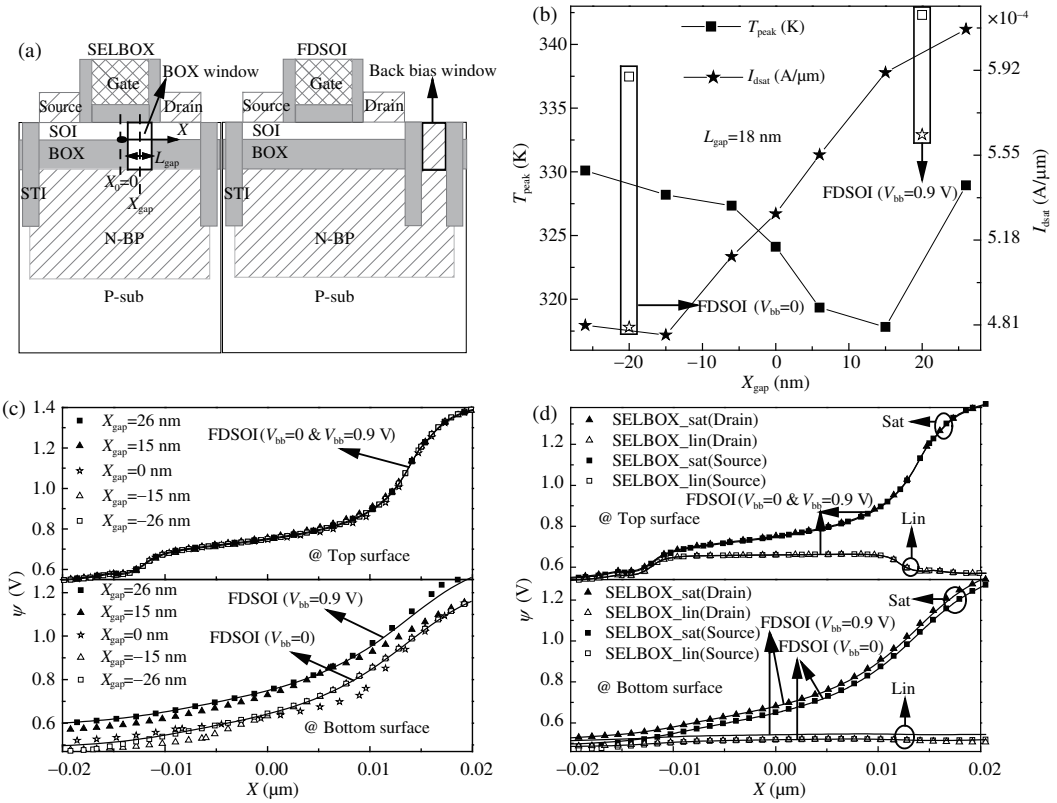

Figure 1 (a) Structures of the SELBOX and FDSOI MOSFETs; (b) thermal and DC performance in different devices; (c) electrostatic potential distributions on the top and bottom surfaces in different devices in the saturation state; and (d) electrostatic potential distributions on the top and bottom surfaces in different devices in linear and saturation states.

are aligned, yield the best results both in terms of the thermal and DC performance. Such an arrangement has great potential for application in integrated circuits. In actual manufacturing, it is difficult to align the active region with the BOX window with reasonable accuracy. However, this process can be made easier if the goal is to place the BOX window near the drain side. This goal can be realized by ensuring that the gate is formed such that it is aligned with the BOX window and by ensuring a small X direction overlay.

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