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• **Supplementary File** •

A High-Efficiency, High Harmonic Rejection E-band SiGe HBT Frequency Tripler for High-Resolution Radar Application

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1 Appendix A

Process Characteristics: The tripler is realized in a Global Foundries 8HP 0.13 μm SiGe BiCMOS technology, featuring a f_T of 200 GHz and a f_{MAX} of 250 GHz. This process offers five thin-metal layers (Metal 1-4, Metal MQ) and two thick-metal layers (Metal LY and Metal AM), as shown in Fig. 1(a). The transmission lines utilize the thickest top metal AM layer and the ground shielding layer of metal MQ to form a ground-shield coplanar waveguide (G-CPW) configuration. Dielectric (SiO_2) thickness between the two metal layers equals 9.62 μm and the G-CPW are modeled using EM simulation.

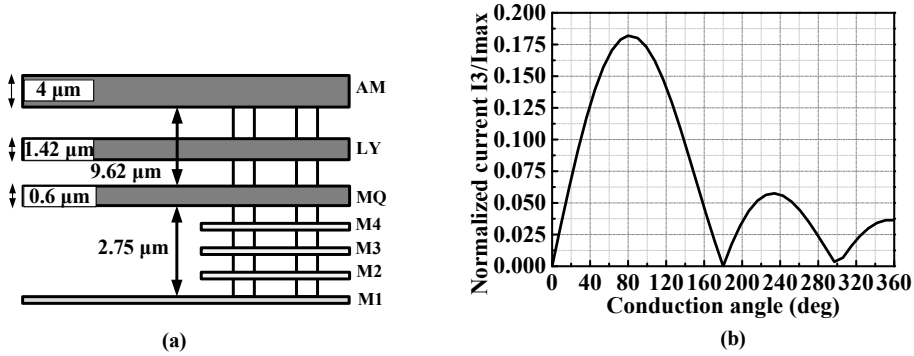

Figure 1 (a) Cross-sectional view of the metal layers, and (b) Normalized third harmonic current as function of conduction angle.

2 Appendix B

Large Signal Analysis of Tripler: Referring to [1], The harmonic component of collector current of the tripler core is a function of conduction angle and determined by the input power level and base bias

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point. For a fixed input sinusoidal base voltage, the collector current can be represented as a train of rectified cosine pulses using a Fourier-series expansion

$$\begin{aligned} I_c(t) =& I_0 + I_1 \cos(w_0 t) + I_2 \cos(2w_0 t) \\ &+ \cdots + I_n \cos(nw_0 t) \end{aligned} \tag{1}$$

where for n=3

$$I_3 = \frac{4I_{max}}{\pi} \cdot \frac{t_0}{T} \cdot \left| \frac{\cos\left(\frac{3\pi t_0}{T}\right)}{1 - \left(\frac{6t_0}{T}\right)^2} \right| \tag{2}$$

I_{max} is the peak collector current, T is the period of the input excitation and t_0 is the time duration of current pulses. Fig. 1(b) illustrates a plot of the normalized harmonic currents I_3/I_{max} as a function of the conduction angle. Thus, in order to achieve maximum third harmonic current, the conduction angle should be around 80^0. By biasing the base current I_B, the desired time duration t_0 can be obtained and thus the optimum condition can be obtained [2]. In this design, the input power is 2 dBm and the static dc bias current is set to be 2.5 mA to maximum conversion gain and output power.

3 Appendix C

Temperature Compensation Design: For most E-band applications, such as WLAN and FMCW, it is desired that the system can function well with moderate performance degradation over temperature variations. In our design, the topology of tripler core was cascode configuration, while the buffer topology was CE configuration. In order to enrich the harmonic signal spectrum, the tripler core was biased in nonlinear status. Buffer stage was biased by the need to elevate the PAE at reduced power levels. Both of them can achieve good efficiency at those levels by employing moderate quasi-static current levels to maximize the performance. However, the current can cause linearity problems because the current can be reduced to nearly zero at low temperature (-40 °C) and increased to several times the room temperature (25 °C) at high temperature (125 °C). Therefore, a temperature compensation based bias circuit was proposed in this design as shown in Fig. 2 to compensate for variation in the quasi-static current which is caused by temperature variation. Since the emitter junctions of transistor Q_1 and Q_3 are tied together,

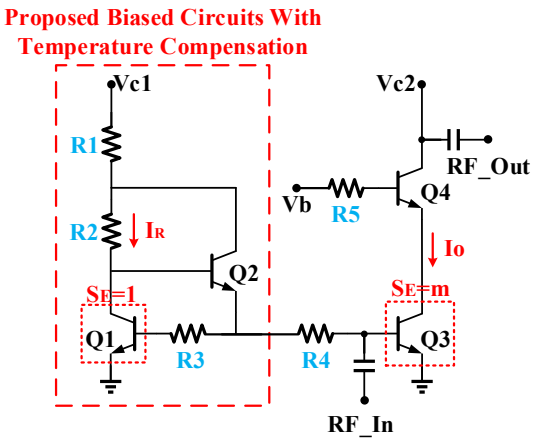

Figure 2 Schematic of the proposed bias circuit with temperature compensation.

that is v_{BE1}=v_{BE3} (voltage drop on R_3 and R_4 can be ignored). Therefore, when they work in active region and ignoring base width modulation effects, there must be

$$I_0 = i_{C3} = (I_{S3}/I_{S1}) i_{C1} \tag{3}$$

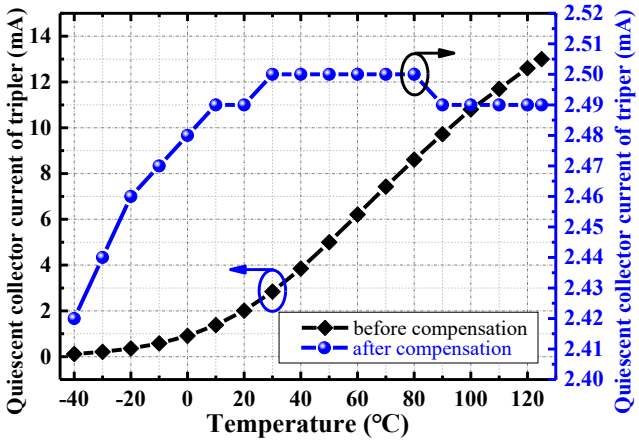

Figure 3 Quiescent collector currents of tripler core before and after temperature compensation.

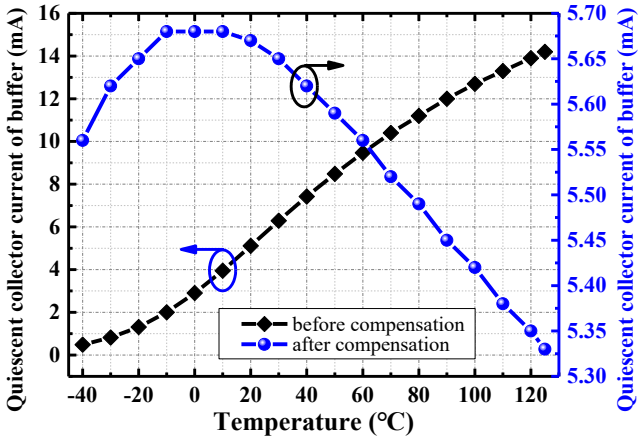

Figure 4 Quiescent collector currents of buffer stage before and after temperature compensation.

Because the saturatuin current I_S is proportional to the emitter area S_E of the transistor, then (3) can be expressed as

$$I_0 = i_{C3} = (S_{E3}/S_{E1})i_{C1} = mi_{C1} \tag{4}$$

In addition, according to the relationship between the base, collector and emitter current of a transistor, it can be obtained that

$$I_R = i_{C1} + i_{B2} \tag{5}$$

$$I_0 = i_{C3} = (I_{S3}/I_{S1})i_{C1} \tag{6}$$

$$(1 + \beta_2)i_{B2} = i_{B1} + i_{B3} \tag{7}$$

$$I_0 = i_{C3} = \beta_3 i_{B3} \tag{8}$$

Furthermore, for the same process it is assumed that

$$\beta_1{=}\beta_2{=}\beta_3{=}\beta \tag{9}$$

Then I_0 can be simplified as

$$I_0 = m \cdot \frac{\beta^2 + 2}{\beta^2 + \beta + 2} \cdot I_R \approx m \cdot I_R \tag{10}$$

From (10), it can be seen that I_0 is determined when I_R is fixed. Besides, by utilizing the current amplification function of Q_2, current $i_{B1}+i_{B3}$ shunt to I_R is significantly reduced. Thus, current i_{C1} is closer to I_R, thereby efficiently reducing the error introduced by the finite β value during the conversion of I_R to I_0. To verify the validity of the proposed temperature compensation bias circuit, the simulated results are compared with those of the uncompensated tripler core and buffer stage, which has the same quiescent collector currents without the compensation circuit in Fig. 2 and the comparison results are shown in Fig. 3 and Fig. 4. As illustrated in Fig. 3, the uncompensated tripler core has quiescent collector current of 2.5 mA at room temperature, and it varies from 117 μA to 13 mA as the temperature changes from -40 °C to 125 °C. However, the quiescent collector current compensated tripler core changes from 2.4 mA to 2.5 mA over the same temperature ranges. Additionally, quiescent collector current of the buffer stage also improved greatly after compensation as plotted in Fig. 4. Moreover, the proposed temperature compensation circuit only requires very small chip area.

4 Appendix D

Measurement Setup of Tripler: The tripler was measured via on wafer probing at temperature ranging from -40 °C to 125 °C, with bonding-wire to dc pad to supply dc power. Two on-wafer test setups were used to measure the third harmonic output frequency and power respectively, as shown in Fig. 5. The measurement setup contains signal generator (Keysight E8257D), power meter (Keysight N1914A) with corresponding power detector, E-band harmonic mixer (OML N9029AE12) and spectrum analyzer (Keysight N9030A). Besides, frequency of fundamental and second harmonic were analyzed using two configuration types: (1) N9030A spectrum analyzer for fundamental and (2) a V-band harmonic mixer and N9030A spectrum analyzer for second harmonic.

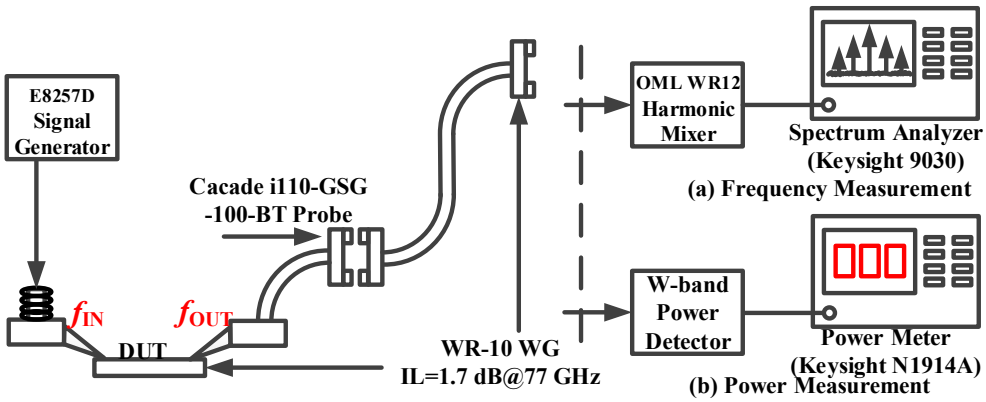

Figure 5 Measurement setup of the tripler.

5 Appendix E

Comparison with State-of-the-Art Frequency Triplers: Table 1 summarizes the published triplers with similar frequency range. Compared with previous work, this tripler demonstrates moderate output power, highest PAE, largest fundamental and second harmonic rejection and function well between -40 °C to 125 °C.

Table 1 Comparison of state-of-the-art frequency triplers

Reference	[3] 2017 MWCL	[4] 2012 MTT	[5] 2016 MWCL	[6] 2015 IMS	[7] 2013 MTT	[8] 2011 MTT	[9] 2013 MTT	**This work**
Process	90nm CMOS	0.18μm SiGe	65nm CMOS	0.13μm SiGe	90nm CMOS	0.15μm mHEMT	65nm CMOS	**0.13μm SiGe**
Type	Tri.+Amp.	PLL+Tri.	Tri.+Amp.	Tri.+Amp.	ILFT	Tri.	x9+Amp.	**HHRT**
Frequency[GHz]	51-70	90-101	57-78	48-58	94	58.5-65	88-99.5	**75-84**
3dB BW[%]	31.5	10.9	31.3	19	3.6	10.5	12.2	**11.7**
Pin[dBm]	4	0	-5	0	6	-1	13	**2**
Pout[dBm]	1.8	-10.5	-2	9.5	-28	-2.6	8.5	**6.8**
PAE[%]	3.42	0.13	1.05	4.05	0.05	0.98	1.62	**7.3**
Fund_Rej[dBc]	>30.8	>20	>20	>28	>23	>20	>31	**>44**
2nd_Rej[dBc]	>35.5	>20	>20	>36	>30	>20	>31	**>45**
Pdc[mW]	44.3	75	60	220	3	56	438	**65.5**
Area[mm^2]	0.92	1.9	0.45	0.94	0.49	2	0.45	**0.89**

References

1 A. Boudiaf; D. Bachelet; C. Rumelhard. A High-Efficiency and Low-Phase-Noise 38 GHz pHEMT MMIC Tripler. IEEE Trans. Microw. Theory Techn , 2000, 48: 2546-2553

2 L. Wang; Y.-Z. Xiong; B. Zhang; S.-M. Hu; T.-G. Lim. Millimeter-Wave Frequency Doubler with Transistor Grounded-Shielding Structure in 0.13 μm SiGe BiCMOS Technology. IEEE Trans. Microw. Theory Techn , 2011, 59: 1304-1310

3 M.-L. Chou, H.-C. Chiu, H.-L. Kao, F.-H. Huang. A 60-GHz CMOS Frequency Tripler with Broadband Performance. IEEE Microw. Wireless Cmopon. Lett , 2017, 27: 281-283

4 C.-C. Wang, Z. Chen, P. Heydari. W-Band Silicon-Based Frequency Synthesizers Using Injection-Locked and Harmonic Triplers. IEEE Trans. Microw. Theory Techn , 2012, 60: 1307-1320

5 Y.-T. Lee; Y.-H. Hsiao; H. Wang. A 57-78 GHz Frequency Tripler MMIC in 65-nm CMOS. IEEE Microw. Wireless Cmopon. Lett , 2016, 26: 723-725

6 N. Mazor; O. Katz; R. Carmon; R. Levinger; A. Bruetbart; D. Elad. A high suppression frequency tripler for 60 GHz transceivers. IEEE MTT-S International Microwave Symposium(IMS), 2015, 1: 1-4

7 Y.-L. Yeh; H.-Y. Chang. A W-Band Wide Locking range and Low DC Power Injection-Locked Frequency Tripler Using Transformer Coupled Technique. IEEE Trans. Microw. Theory Techn , 2013, 61: 860-869

8 N.-C. Kuo, J.-C. Kao, Z.-M. Tsai, K.-Y. Lin, and H. Wang. A 60-GHz Frequency Tripler with Gain and Dynamic-Range Enhancement. IEEE Trans. Microw. Theory Techn , 2011, 59: 660-671

9 N. Mazor, and E. Socher. Analysis and design of an X-banto-W-band active multiplier with improved harmonic rejection. IEEE Trans. Microw. Theory Techn , 2013, 61: 1924-1933