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Single-event upset prediction in static random access memory cell account for parameter variations

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Dear editor,

As technology downscales, the impact of process variations (PVs) becomes a harmful problem, which significantly affects the integrated circuit (IC) performance [1]. The transistor parameters can be significantly affected by the lithography, random dopant fluctuations (RDFs), surface-state charge, gate depletion, and line edge roughness [1, 2].

BSIM4-based Monte Carlo (MC) simulations induced a qualitative and quantitative analysis method to measure the contribution of PVs to transistor parameter response and obtain the SE response. The entire and individual parameter variations can be obtained during the BSIM4 MC simulations. The parameter variations can significantly affect the single-event upset (SEU) and SEU recovery in static random access memories (SRAMs) and flip-flop circuits. In combinational logic, parameter variations can induce SET and SET quenching shifts [3–5].

SEU prediction needs accurate charge collection quantization, but PVs will affect the SE response. As a result, it is very important to study how SEU prediction is affected by parameter variation. In this study, a novel SEU cross-section calculation method is proposed to study the relationship between the parameter variations and SEU cross-section. To the best of our knowledge, this relationship has not been studied before.

Simulation methods for SEU prediction. Herein, a 6-T (6 transistors) typical SRAM circuit is used for SEU prediction and its layout is generated by a memory compiler, which is based on a 65-nm complementary metal-oxide-semiconductor (CMOS) process design kit (PDK). TCAD transistor models are built according to the SRAM layout information. In TCAD mix-mode simulation, the cross-coupled transistors (i.e., the core transistors of the cell) are implemented by TCAD; other transistors are implemented in SPICE codes.

Heavy-ion simulations are implemented by the radiation model. A heavy-ion-induced current can be saved into PWL style files and injected into the Spectre circuit simulation tool. In total, 10000 MC simulations are conducted for each ion strike. To precisely represent the long-time manufacturing performance, all parameters are varied according to the BSIM4 MC PDK; the parameter variation is global so that local mismatch is not included. SEU probability is calculated by the number of ion strikes divided by the upset numbers.

PV can significantly affect a transistor's physical and electrical parameters as well as the single-event response. When the ion strikes the SRAM, the charge collection amount changes along with the parameter variations. For no-parameter cases, the off-transistor critical charge ($Q_{\rm crit}$) is fixed. When the charge collection amount is larger than or equal to $Q_{\rm crit}$, SEU will occur in SRAM. When

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the charge collection amount is less than $Q_{\rm crit}$, SEU cannot be observed. However, when considering the case of parameter variation, $Q_{\rm crit}$ is affected by parameter shifts. Furthermore, for a range of collected charges, SEU shows a probability distribution.

To study the impact of parameter variation on SEU, TCAD heavy-ion simulations are conducted on NMOS and PMOS transistors. $Q_{\rm crit}$ values of NMOS and PMOS are obtained after heavy ions with different LET values vertically striking on the surface. The simulation results reveal that the $Q_{\rm crit}$ values of NMOS and PMOS transistors (65-nm technology) are 6.7 and 10.95 fC, respectively. The drain current curves simulated from TCAD are saved into PWL style files. In Spectre MC parameter variation simulations, the PWL files are injected as drain current sources.

In total, 10000 simulations are conducted for each drain current source. Information such as SEU numbers, charge collection amount, and transistor parameters can be collected to analyze the relationship between charge collection amount and SEU probability. The results are presented in Figure 1(a) and (b). The results have a trend same as that of the simulation results of a previous study [2].

Simulation methods for parameter variation. In Figure 1(a) and (b), minline and maxline are defined as the boundaries of the parameter variation impact on SEU. When the charge collection amount is above maxline, the SEU probability is 100%; however, when the charge collection amount is below minline, the SEU probability is zero. The actual impact of parameter variation on SEU can be determined from the simulation data between minline and maxline. In other words, at the charge collection amount data point in the PV sensitive region, when $Q_{\rm coll} > Q_{\rm crit}$, the SEU probability is not 100%. Following the same line of reasoning, when $Q_{\rm coll} < Q_{\rm crit}$, the SEU probability is not zero and the SEU event probability is equal to the SEU probability in the PV region.

Assume that S is the area of the SRAM cell; n_i and m_i represent the number of ions striking on the off-transistor and on-transistor, respectively; M is the event number of ions striking the off-transistor SV; and N is the event number of ions striking the on-transistor SV. The SEU cross-section accounts for PV can be calculated as follows:

$$\sigma_{\rm SP} = \frac{S}{N_i}\sum_{i=1}^{N} n_i - \frac{S}{M_i}\sum_{i=1}^{M} m_i, \tag{1}$$

where $\sigma_{\rm SP}$ is SEU cross section account for PV, and S is the total number of simulations, and n_i and m_i are calculated from (2) and (3), respectively.

$$n_i = \begin{cases} 0, & Q_{\rm n,poff} < \text{minline}, \\ 1, & Q_{\rm n,poff} > \text{maxline}, \\ P_{\rm SEU}, & \text{minline} \leqslant Q_{\rm n,poff} \leqslant \text{maxline}, \end{cases} \tag{2}$$

$$m_i = \begin{cases} 0, & Q_{\rm n,pon} < Q_{\rm critn,pon}, \\ 1, & Q_{\rm n,pon} \geqslant Q_{\rm critn,pon}, \end{cases} \tag{3}$$

where $i = 1, 2, \ldots, N$. $Q_{\rm n,poff}$ and $Q_{\rm n,pon}$ are off-transistor and on-transistor charge collection amount and on-transistor charge collection amount of NMOS(N) and PMOS(P) FETs, respectively. $Q_{\rm critn,pon}$ is the on-NMOS and on-PMOS Qcrit for SEU recovery. $P_{\rm SEU}$ is the SEU probability that can be obtained from (2), and the value is determined from Figure 1(a) and (b).

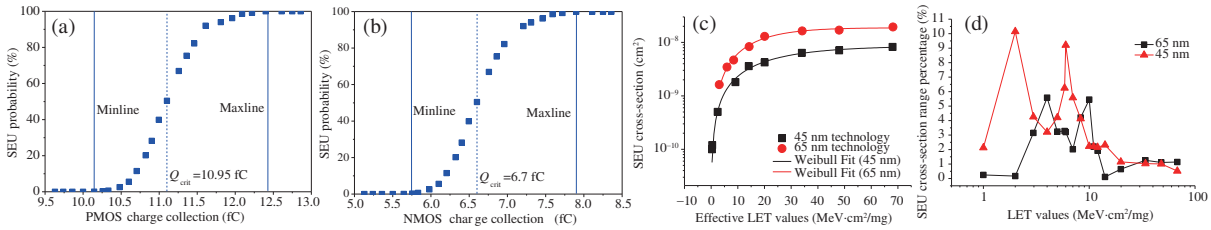
65 nm simulation results. Figure 1(e) shows the SEU cross-section, and the shift ranges between the case with PV and the case without PV. According to a method discussed in previous researches [2, 4, 5], we propose a parameter named "SEU cross-section range percentage" to study the SEU cross-section shift accounts for PV. This parameter is used to quantify how PV affects SEU, which will improve the accuracy of SEU cross-section prediction when considering PV.

The simulation results in Figure 1(e) show that PV may induce 5.28% SEU cross-section shifts and that most level shifts occur when the effective LET value is 5.85 MeV cm^2/mg. The reason is that the charge collection of the sensitive volume approach to SEU $Q_{\rm crit}$, then the affection of sensitive volume mostly occurs near the $Q_{\rm crit}$ region.

45 nm simulation results. Simulations are also conducted on a 45-nm technology process. The Qcrit values of NMOS and PMOS transistors are simulated by TCAD, and simulation results show that the smaller transistor has a correspondingly smaller $Q_{\rm crit}$ (1.98 fC of NMOS $Q_{\rm crit}$ and 5.89 fC of PMOS $Q_{\rm crit}$). This means that the single-event effect is more sensitive for the dual-well 45-nm technology than it is for the 65-nm technology.

Similar to a previous study [3], the sensitive volumes are calibrated by TCAD mixed-mode simulations. The simulation results of Off-NMOS and Off-PMOS SVs show that compared with 65-nm transistors, 45-nm transistors have smaller SVs and charge collection coefficients.

The SEU cross-section simulations are performed using the proposed SEU prediction tools. The heavy ions and LET values are the same as those considered in a previous study [3]. The simulation results and Weibull fit curves are presented in Figure 1(c).



(e)

Particles	Z	A	Energy (MeV)	Angle (°)	Effective LET values (MeV·cm²/mg)	SEU Cross section without PV (cm²)	SEU Cross section account for PV (cm²)	SEU Cross section variation range percentage (%)
N^{4+}	7	15	139	0	2.97	1.608×10^{-9}	1.557×10^{-9}	3.15
Nc^{6+}	10	20	786	0	5.85	3.4848×10^{-9}	3.301×10^{-9}	5.28
				45	8.3	4.672×10^{-9}	4.615×10^{-9}	4.21
Ar^{12+}	13	40	372	0	14.1	8.3984×10^{-9}	8.389×10^{-9}	0.11
				45	19.9	1.304×10^{-8}	1.295×10^{-8}	0.65
Kr^{22+}	36	82	768	0	34	1.66×10^{-8}	1.639×10^{-8}	1.26
				45	48	1.7488×10^{-8}	1.699×10^{-8}	2.81
Xc^{35+}	54	131	1217	0	68	2.0064×10^{-8}	1.943×10^{-8}	3.14

Figure 1 (Color online) Simulation results. (a) SEU probabilities for PMOS charge collection in 65-nm SRAM; (b) SEU probabilities for NMOS charge collection in 65-nm SRAM; (c) comparison of SEU cross-section for the 65- and 45-nm SRAMs; (d) SEU cross-section range percentage for the 65- and 45-nm transistors; (e) SEU cross-section shifts induced by parameter variations in 65-nm simulations.

From Figure 1(c), we can see that the cross-section of the 45-nm transistor is significantly smaller than that of the 65-nm transistor. As stated previously, in comparison with the 65 nm transistor, the 45-nm transistor is more sensitive to striking ions. However, as technology scale, the area of the cell is shirking and the area of cell is smaller for the advanced technology. As a result, the cross-section per unit in the 45-nm transistor is smaller than that in than 65-nm transistor.

The data in Figure 1(d) indicate that the effect of PV on the SEU cross-section is more significant in the 45-nm transistor than it is in the 65-nm transistor. In the 45-nm transistor, the SEU cross-section range percentage is more than 10%, which will significantly affect the accuracy of SEU predictions. The peak points for the dual-well 65- and 45-nm transistors are near the NMOS and PMOS Qcrit regions.

The SEU prediction platform (based on TCAD simulation, parameter variation MC simulations, and Geant4 simulations) used herein is described more comprehensively in a previous study [6]. The nested and on-transistor SVs are used in order to quantify the charge collection and sharing, and thus, the PV simulations in this study consider the charge sharing and recovery.

Conclusion. In this study, simulations were conducted on dual-well 65- and 45-nm CMOS SRAM cells to study the effect of parameter variation on the SEU cross-section. The results indicated that parameter variation could significantly affect the SEU cross-section. For 65-nm transistors, parameter variation may induce an SEU cross-section shift of more than 5%, whereas for 45-nm transistors, parameter variation induces an SEU cross-section shift of more than 10%. Therefore, it is necessary to consider parameter variation when calculating the SEU cross-section.

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