SCIENCE CHINA
Information Sciences

• LETTER •

June 2019, Vol. 62 069402:1–069402:3
https://doi.org/10.1007/s11432-017-9549-8

Dependency of well-contact density on MCUs in 65-nm bulk CMOS SRAM

Cheng XIE*, Yueyue CHEN, Jianjun CHEN & Jizuo ZHANG

College of Computer, National University of Defense Technology, Changsha 410073*, China*

Received 12 November 2017/Revised 22 March 2018/Accepted 14 August 2018/Published online 22 October 2018

Citation Xie C, Chen Y Y, Chen J J, et al. Dependency of well-contact density on MCUs in 65-nm bulk CMOS SRAM. Sci China Inf Sci, 2019, 62(6): 069402, https://doi.org/10.1007/s11432-017-9549-8

Dear editor,

In custom static random access memory (SRAM) cell, radiation-induced single bit upsets (SBUs) are considered as the main cause of soft error [1]. Advanced technologies and scaling down of feature sizes have made single-event multiple cell upsets (MCUs) as the vital source of soft error for SRAM [2]. Moreover, under certain single particle hitting conditions, single event transient (SET) at periphery circuit and single event latch-up (SEL) appearing in the circuit, can affect MCU as well [3]. MCU induced by single event effect, which may cause SRAM logical confusion and subsequently permanent failure, has been widely reported. Therefore, it is important to study the hardening technique to mitigate MCU on SRAM radiation-induced bipolar effects dominantly induce MCU [4], and MCU rate depends on well-contact density. Well-contact structure is widely used in SRAM owing to its capability to keep the well potential stable and avoid well potential collapse. Thus, high density of well-contacts can greatly decrease MCU occurrence in SRAM.

In this study, the impact of well-contact density on SRAM is analyzed using heavy-ion radiation experiment. Two hardened SRAM chips designed with high density well-contacts are fabricated in a 65-nm bulk CMOS technology. MCU characterizations of a common commercial and two hardened SRAM are compared and discussed. In addition, the MCU characterizations of the two hardened chips designed with different cell densities are also studied.

Experimental chips. In this experiment, a custom SRAM C and two hardened SRAM, namely, SRAM A and SRAM B, are fabricated in 65-nm bulk process to measure upsets. Custom chip has low density well-contacts, while hardened chips have high density well-contacts.

All the experimental chips use storage array interleaving distance (ID) scheme with EDAC code to eliminate the influence of the MCUs [4,5], which occurs in the different logical words. Compared to the traditional layout, this layout does not increase the number of transistors and performance overhead but increases the difficulty of metal wire interconnection, significantly reduces the number of MCUs generated by adjacent logic cells, and effectively prevents the circuit logic from being invalid. In addition, the two hardened chips have different densities of sensitive nodes. A sensitive node is the drain of a turned-off transistor, and is usually the area where the data are stored, charge can be easily collected after single-particle hit. The distance between two adjacent sensitive nodes is larger in SRAM A than that in SRAM B. Hence, SRAM A has lower sensitive node density than SRAM B.

Experimental process. The initial storage array model was first taken into account. All the SRAMs use "checkerboard" setup. It has been reported that "checkerboard" setup can reduce the occurrence of MCUs in adjacent row cells [6]. Further-

* Corresponding author (email: xcv61988539@163.com)

© Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

(a)

Ion	Chip	1 bit	2 bit	10 bit	SEL
Ge	A	608	0	0	0
	B	663	0	0	0
	C	799	0	0	0
Ti	A	593	0	0	0
	B	650	0	0	0
	C	527	0	0	0
O	A	112	0	0	0
	B	165	0	0	0
	C	92	9	0	0

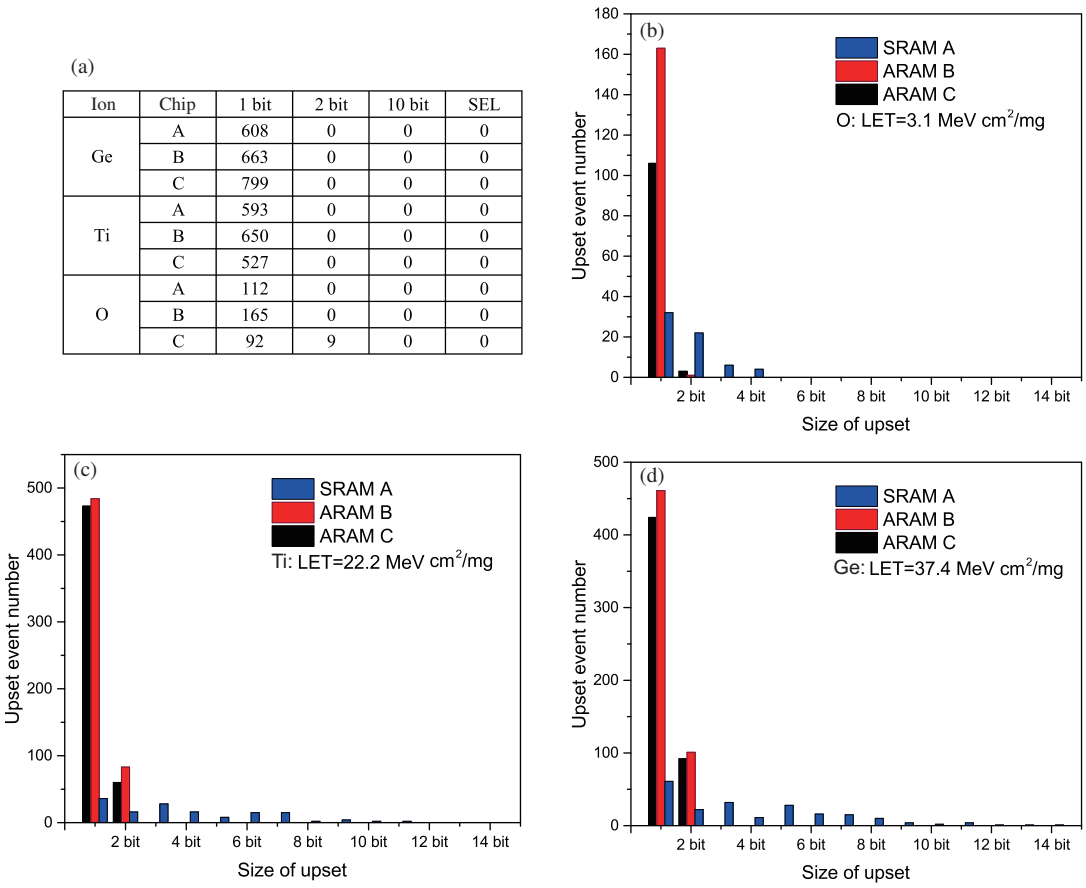

Figure 1 (Color online) (a) Upset in logical word of SRAM in the experiments. The size of upset in physical address on three SRAMs in the experiments at O exposure (b), at Ti exposure (c), and at Ge exposure (d).

more, some studies have shown that the distribution of MCUs primarily depends on the distribution of the off-state transistors in adjacent memory cells [7]; charge can be easily collected in these regions.

Radiation tests for the experiments were performed using the HI-13 tandem accelerator in the China Institute of Atomic Energy, Beijing. Three different linear energy transfers (LET) of particle were broguht into use. They are O (LET = 3.1 MeV cm^2/mg), Ti (LET = 22.2 MeV cm^2/mg), and Ge (LET = 37.4 MeV cm^2/mg), respectively. Incident angle of radiation is 90°. To ensure that these particles hit each sensitive node to the maximum extent, we measured and counted SBUs, MCUs, and upset sections after 3×10^7 ions/cm^2 strikes.

Experimental results and discussion. The logical upsets data of 65-nm SRAM in the experiments for three heavy ions is tabulated in Figure 1(a). There was no evident change in the value of current in three chip types in the experiment, so these chips did not appear to exhibit any latch-up, thus, the threshold value of amount of LET to cause SEL is definitely higher than 37.4 MeV cm^2/mg. A large number of single event upsets (SEUs) were generated in three chips. As the LET value of the irradiated particles increased, the number of upsets increased. Besides, through storage array ID scheme, the physical adjacent cells were distributed into different logical words. However, there are still several multiple bit upsets present in SRAM C. Hence, it is essential key to explore the actual upsets in physical address.

In order to evaluate the multicell upsets in actual physical address caused by the three single particles, the upsets data at the particular physical address are recorded as depicted in Figure 1(b)–(d). Charge sharing is the main reason for occurrence of MCU, and there are two main reasons for charge sharing, namely bipolar effect and charge diffusion. A large number of continuous upsets in commercial chip C occur along the direction of the well and with the increase in LET, the total number of upsets and bits of upsets increase up to 14-bit upsets. A large number of MCUs occur in SRAM C. In contrast, hardened SRAM A/B with high density well-contact did not induce a large area of the multiple cell upsets after particle radiation, but induced only 2-bit upsets in the vertical

direction of the adjacent cells. Hence, compared to the low density well-contact structure, the high density well-contact structure can more effectively maintain a stable well potential and avoid well potential collapse, which leads to suppression of the bipolar effect resulting in less charge collection in hardened SRAM. Therefore, it can be concluded that number of MCUs on an SRAM is drastically reduced by using a high density well-contact structure.

In addition, the hardened chips A and B were also studied in the experiment. As mentioned earlier, SRAM A has lower sensitive node density than SRAM B. Closeness of cell pairs can increase charge sharing [4], but closeness to well-contact can suppress bipolar effect between cell pairs. Thus, SRAM A has stronger bipolar effect but weaker charge diffusion effect. Under the radiation of low-energy O particle, SRAM A produces larger number of MCUs than SRAM B, so the bipolar effect at low LETs is the main mechanism for SRAM A to produce larger number of MCUs. However, in heavy ion radiation experiments, in which Ti and Ge were used with higher LETs, the number of MCUs appearing in SRAM A is less than that in SRAM B so indicating that charge diffusion is the main mechanism for the occurrence of MCUs in this case. The experimental data of two hardened chips shows that the number of total bit upsets in chip A is less than those in B for all the three heavy ions. This indicates that charge sharing by diffusion has more marked effects on total bit upsets when bipolar effect is mitigated efficiently by high density well-contacts. Thus, a higher well-contacts density with a larger sensitive node density has a better performance in MCU mitigation. Our study further indicated that the upsets in one logical word can be completely eliminated by this hardened design technique using the storage array interleaving distance scheme and EDAC codes.

Conclusion. A common commercial chip with low density well-contact and two hardened chips with high density well-contact were fabricated in a 65-nm bulk CMOS technology. The characterization of MCUs in the custom and hardened SRAM was performed. The effect of well-contact density on MCU was studied in-depth through heavy ion experiments, for which O, Ti, and Ge particles were used. Experiment results also show that the number and bit of MCU on SRAM can be reduced drastically by increasing the well-contact density. Common commercial chip was found prone to inducing MCU and a maximum of 14 cell upsets occured in it while hardened-chips had only a maximum of 2 cell upsets. The two hardened SRAM, which had higher sensitive node density, performed better. It is worth noting that MCUs on the same logical word can be completely eliminated by this hardened design technique using the storage array interleaving distance scheme and EDAC codes.

Acknowledgements This work was supported by Preliminary Research Program of National University of Defense Technology of China (Grant No. 0100066314001).

References

1 Chen J J, Liang B, Chi Y Q. Experimental characterization of the bipolar effect on P-hit single-event transients in 65 nm twin-well and triple-well CMOS technologies. Sci China Technol Sci, 2016, 59: 488–493
2 Chatterjee I, Narasimham B, Mahatme N N, et al. Impact of technology scaling on SRAM soft error rates. IEEE Trans Nucl Sci, 2014, 61: 3512–3518
3 Luo Y H, Zhang F Q, Guo H X, et al. Single-event cluster multibit upsets due to localized latch-up in a 90 nm COTS SRAM containing SEL mitigation design. IEEE Trans Nucl Sci, 2014, 61: 1918–1923
4 Zhang K Y, Kobayashi K. Contributions of charge sharing andbipolar effects to cause or suppress MCUs on redundant latches. In: Proceedings of IEEE International Reliability Physics Symposium, 2013
5 Jeon S H, Lee S, Baeg S, et al. Novel error detection scheme with the harmonious use of parity codes, well-taps, and interleaving distance. IEEE Trans Nucl Sci, 2014, 61: 2711–2717
6 Ibe E, Chung S S, Wen S J, et al. Spreading diversity in multi-cell neutron-induced upsets with device scaling. In: Proceedings of IEEE Custom Integrated Circuits Conference, 2006. 437–444
7 Gasiot G, Roche P, Flatresse P. Comparison of multiple cell upset response of bulk and SOI 130 nm technologies in the terrestrial environment. In: Proceedings of IEEE International Reliability Physics Symposium, 2008