SCIENCE CHINA
Information Sciences

• NEWS & VIEWS •

June 2019, Vol. 62 067401:1–067401:2
https://doi.org/10.1007/s11432-019-9873-x

International Solid-State Circuits Conference 2019 aims at "envisioning the future"

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Received 25 March 2019/Accepted 18 April 2019/Published online 7 May 2019

Citation Jia H K, Chi B Y. International Solid-State Circuits Conference 2019 aims at "envisioning the future". Sci China Inf Sci, 2019, 62(6): 067401, https://doi.org/10.1007/s11432-019-9873-x

The International Solid-State Circuits Conference (ISSCC) is well known as the best global forum with respect to solid-state circuits and systems-on-a-chip. Held in San Francisco in January or February each year, the conference attracts more than 3000 researchers and engineers from academia as well as industry worldwide to discuss cutting-edge IC designs, exchange advanced technique ideas, and network with their peers.

Driven by Moore's Law, the semiconductor industry has enjoyed more than 30 years of high-speed expansion. In the past, people could expect the same design to have improved performance and efficiency year after year, taking advantage of the scaling of process technology. This situation is no longer true. The process-technology scaling path is not sustainable anymore, and it has become increasingly challenging to catch up with the pace predicted by Moore's Law. The challenge arises from both technology and economic perspectives. These challenges have provided the motivated to explore new possible paths to the further development of the semiconductor industry. Innovations are needed at different levels—from devices and integration techniques, to system architecture, original approaches, and new applications such as IoT and 5G. The ISSCC 2019 is aimed at driving innovation that will inspire future development. So, the theme of ISSCC 2019 is "envisioning the future."

Covering almost all research topics in the field of solid-state circuits and systems, the conference includes several specific topics that draw considerable attention.

Research in the fields of neural networks and deep learning seized the spotlight at the conference this year. In the past, progress in this area was found to be greatly influenced by the available hardware [1]. One property of deep learning systems is that when the system becomes larger, the result becomes better. From the perspectives of power consumption and speed, CPUs and GPUs, with their generalized architecture, are in capable of performing computations in large-scale deep learning systems. It is believed processors specific for deep learning are necessary. The ISSCC 2019 included two plenary talks and two sessions on machine learning. These studies pursue innovative architecture to improve the speed and energy efficiency of specific machine-learning chips. The speed of the deep-learning accelerator has been pushed to a new level of 11.5 tera-operation/second (TOPS).

The 5G era is much closer to us than ever. It is not simply an evolution of 4G. As mentioned in [2], 5G will not only optimize human-human communication as in 4G, but also deliver solutions for machine-type communications. Further, 5G raises challenges from the system level to core technologies, including low-power architecture, beamforming techniques, and antenna and RF designs. Studies presented at the ISSCC 2019 include those on a 71–76-GHz large-scale (64-element) phased array in FinFET CMOS process for 5G application

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and several MIMO transceivers working at around 30 GHz.

Ultra-high-speed wireline was another hot topic in this year's ISSCC. Driven by applications such as machine learning, 5G communications, and data centers, the demand for I/O bandwidth is growing rapidly. The wireline transceiver techniques are continuously evolving from 56 Gb/s to 112 Gb/s per line, with the help of process-technology scaling, to meet the I/O bandwidth requirements. Studies presented at the ISSCC 2019 include those on a PAM-4 receiver and transmitter with a data rate greater than 100 Gb/s in 14-nm FinFET technology. Along with pushing the data rate to the limit, researchers are improving both the energy efficiency and signal integrity of the 56 Gb/s generation wireline transceivers. A benchmark sub-250 mW 56 Gb/s ADC/DAC-based PAM-4 transceiver supporting 42.5 dB channel loss was reported in the ISSCC 2019.

Internet of things (IoT) is the next big thing in the semiconductor industry. Low-power sensor technology is the key to enabling IoT. It is believed that the number of IoT devices will exceed 30 billion by 2020. Considering that each IoT device can have several sensors, the number of sensors needed in the IoT era will be huge. To extend battery life, the sensors should function with ultra-low power. For example, the power consumption of a sensor should be less than 650 nW to sustain it for a year when powered by a 5-mm coin-cell battery (2 mAh). Several studies presented in this year's ISSCC were dedicated to further reducing the power consumption of sensors. These studies covered various types of sensors, such as voice and acoustic activity detection sensors, photoplenthysmographic sensors, strain sensors, and neural recording sensors. The power consumption of these sensors can be as low as 142 nW [3].

The conference also dwelt on the newest development in memory devices, both standalone and embedded. It continuous the trend of faster access, larger capacity, and lower power consumption. Several big companies from the industry showcased their advance memory technology at the ISSCC this year. Samsung presented the first device for new DRAM standard LPDDR5. The device has not only a data rate of 7.4 Gb/s per pin, but also 21% and 33% lower power consumption for read and write as compared to the previous-generation devices. SK Hynix has realized a DRAM package with capacities of 512 Gb by combining eight chips together with a controller. With regard to storage, Toshiba has pushed the density of 3D-Flash Memory to 1.33 Tb per chip or greater than 1 Gb per square millimeter.

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