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A 0.45-to-1.8 GHz synthesized injection-locked bang-bang phase locked loop with fine frequency tuning circuits

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Abstract This paper proposes a synthesized injection-locked bang-bang phased-locked loop (SILBBPLL) with high digital controlled oscillator (DCO) frequency resolution. The SILBBPLL is expressed with hardware description language and automatically placed & routed (APR) by using standard digital circuit design flow. As the mismatch issues of the circuits are not considered carefully during the APR design flow, the phase noise performance is severely deteriorated. We adopt pulse injection locking technique to improve the phase noise performance. The DCO frequency resolution is critical for reducing the reference spur in a digital injection-locked PLL. Therefore, we propose novel frequency tuning circuits to increase the DCO frequency resolution so that the reference spurs are reduced. The frequency tuning circuits consist of a standard cell based high-linearity output feedback DAC (OFDAC) and two custom varactors. The OFDAC is used to tune the frequency of the DCO with the custom varactor precisely. The custom varactor is firstly designed, added into the standard cell library, and APR with the standard cells. The SILBBPLL chip with a core area of 0.008 mm^2 is implemented in 65 nm CMOS process. When operating at 1.8 GHz, the measured results show that the root-mean-square (RMS) jitter integrated from 10 kHz to 100 MHz is 1.1 ps, and the power consumption is 1.5 mW with a 0.8-V supply. The proposed SILBBPLL achieves a figure-of-merit (FoM) of −237.4 dB and a reference spur of −50.9 dBc.

Keywords synthesized all-digital phased-locked loops (ADPLL), bang-bang phased-locked loop (BBPLL), automatically placed & routed (APR), output feedback DAC (OFDAC), injection-locked

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1 Introduction

Recently, the performance of digital integrated circuits (IC) keeps improving with CMOS process scaling down. On the other hands, the performance of analog ICs designed with advanced CMOS process are limited by low intrinsic device gains, large leakage current and low supply voltage. Therefore, digital implementations of analog and mixed signal ICs become more and more attractive [1–7].

Phase locked loop (PLL) with low jitter or phase noise is essential for clock generation, data conversion and frequency synthesis [8, 9]. Many all-digital phased-locked loops (ADPLL) have shown better performances in terms of area, power and jitter than the analog PLLs [10–14]. Besides, these ADPLLs

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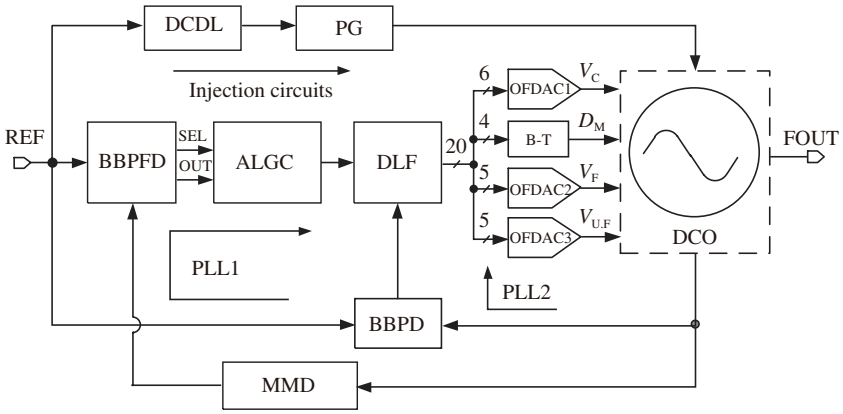


Figure 1 Block diagram of SILBBPLL.

have advantages of scalability and programmability over their analog counterparts. However, they still require heavily manual layout design effort, which takes a long time during the whole design period.

In order to shorten the circuit design cycle, some synthesized ADPLLs were recently proposed [15–24]. Although these synthesized ADPLLs have shown advantages of significantly short design period, they still have problems such as limited frequency tuning resolution, poor phase noise, and large reference spurs. In [15], the synthesized ADPLL was designed and automatically placed & routed (APR) entirely from the commercial standard digital cells, but the frequency resolution of the digital controlled oscillator (DCO) is limited by the minimum capacitance of the standard cells, which result in poor jitter performance. In [16–20], the DCO resolution is improved by manually designing the DCO blocks, but the custom design of the DCO degrades the advantages of the synthesized PLL. In [22, 23], the phase noise performance of the synthesized PLL is improved by adopting edge-injection locking technique. But the injection-edge introduces a large the reference spur at the PLL output.

In this paper, we propose a synthesized injection locked bang-bang phased-locked loop (SILBBPLL) with high DCO frequency resolution. The SILBBPLL is expressed with hardware description language (HDL) and APR by using standard digital circuit design flow. As the mismatch issues of the circuits are not considered carefully during the APR design flow, the phase noise performance is severely deteriorated. We adopt pulse injection-locking technique to improve the phase noise performance. However, if the DCO frequency resolution is poor, a large phase shift will be derived from the injection locking point, which degrades the jitter-reduction effect and it will cause a large reference spur. Therefore, we propose novel frequency tuning circuits to increase the DCO frequency resolution so that the reference spurs are reduced. Transfer curve of the standard cell based digital to analog converters (DACs) is developed and analyzed. The spur reduction effect of the proposed frequency tuning circuits is analyzed and verified with measurement results.

2 Architecture of the proposed SILBBPLL

2.1 Architecture and design methodology

The architecture of the SILBBPLL is presented in Figure 1. It consists of a DCO, three OFDACs (OFDAC1, OFDAC2 and OFDAC3), a binary to thermometer (B-T) converter, injection circuits and two loops (PLL1, PLL2). The PLL1 consists of a multi-modulus divider (MMD), a bang-bang phase/frequency detector (BBPFD) and an adaptive loop gain controller (ALGC). The ALGC in PLL1 is adopted to accelerate the frequency locking process [7]. The PLL2 consists of a BBPD and a digital loop filter (DLF). The BBPD is made of a single dynamic flip-flop (DFF). The injection circuits include a pulse generator (PG) and a digital control delay control line (DCDL). The OFDAC1 is used to control DCO coarse frequency tuning. The OFDAC2 and OFDAC3 are proposed to realize DCO fine and ultra-fine frequency tuning

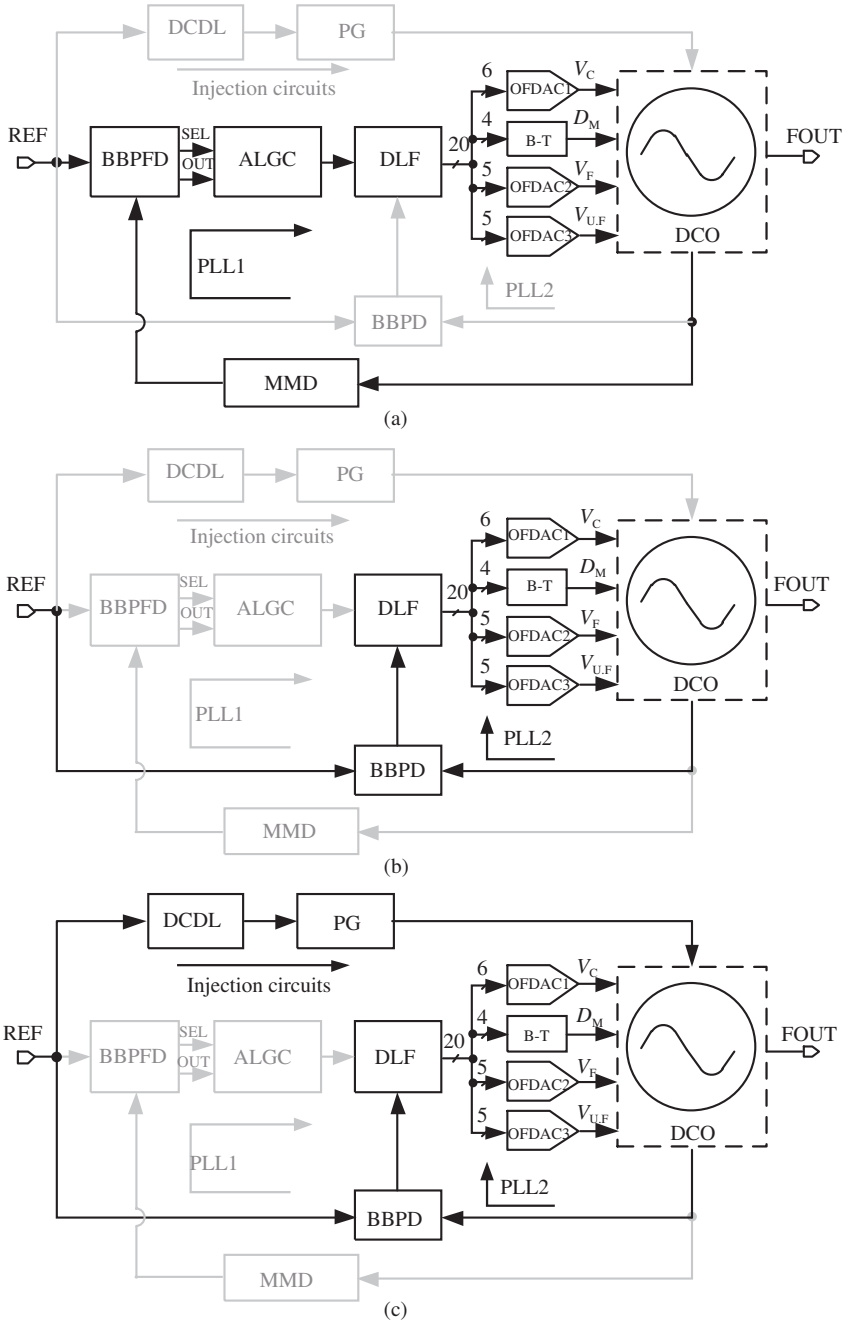


Figure 2 Operating procedure of the SILBBPLL. (a) PLL1 for traditonal frequency and phase locked; (b) PLL2 to reduce the static phase error for injection locking; (c) injection locking.

with the custom varactors, respectively, which will be discussed in details in the following sections. The PG is adopted for the injection locking and DCDL is used for calibrating the injection timing error. With the injection locking, phase noise of the SILBBPLL can be greatly reduced. The SILBBPLL is described with HDL and APR using the standard digital design flow. Compared with the time-to-digital (TDC) based ADPLL, the BBPLL has merits of circuits simplicity and robustness to process variation [25–29]. Therefore, it is very suitable for the design of synthesized PLLs.

The locking process of the SILBBPLL includes the three following operating steps: (1) the frequency and phase locking; (2) phase error elimination and injection timing calibration; (3) injection locking. Figure 2 shows the operating steps of the SILBBPLL. Figure 2(a) shows the first operation step of the frequency and phase locking. The PLL1 is enabled and PLL2 is disabled to make the SILBBPLL locked

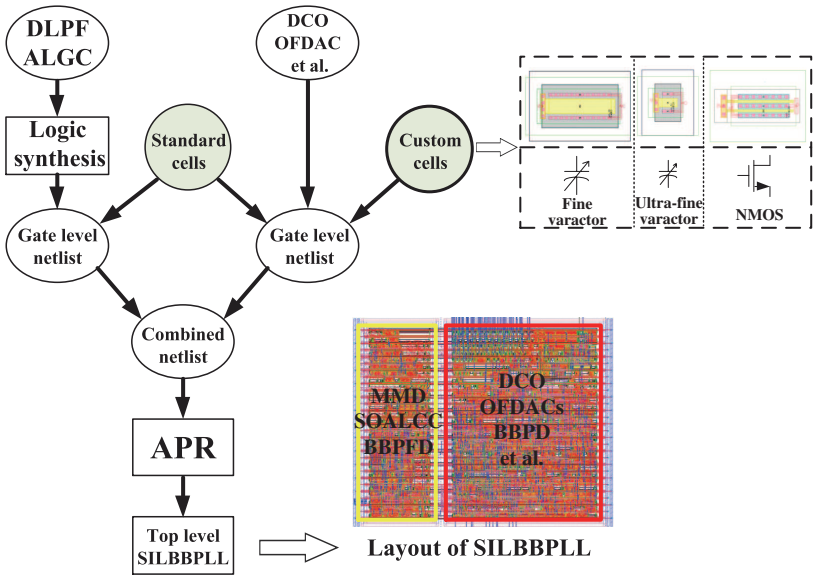


Figure 3 (Color online) Design methodology of the SILBBPLL.

to the target frequency. Figure 2(b) shows the second operation step of the phase error elimination and injection timing calibration. PLL2 is enabled and PLL1 is disabled to reduce the static phase error between the DCO and reference clock. When PLL2 is locked, the static phase error is reduced to one intrinsic DFF delay, thus the injection timing error is calibrated small enough for injection locking [29]. Figure 2(c) shows the third operation step of the injection locking. When the injection timing is well calibrated, the injection locking circuits are enabled to make the SILBBPLL be injection-locked to further improve the phase noise performance. When the SILBBPLL is injection locked, PLL1 is kept disabled to save power. And PLL2 keeps enabled and works as a tracking loop to continuously calibrate the phase drifting of the DCO, caused by the process voltage temperature (PVT) variations [29].

Design methodology of the SILBBPLL is presented in Figure 3. Only two kinds of varactors (fine varactor and ultra-fine varactor) and one NMOS cell are custom designed as standard cells and added to the standard cells library. That is, the timing, layout and routing information (contained in the .LIB, .LEF and .GDS files) of the custom cells are provided to the EDA tools, like the standard cells [2]. The custom cells are designed to have the same vertical pitch as the standard cells. The DCO, MMD, OFDACs are described with gate-level HDL. The ALGC and DLF are designed with register-transfer-level (RTL) HDL. The whole SILBBPLL is then APR using standard digital circuit design flow. The MMD, BBPFD and ALGC are APR as a macro in the SILBBPLL, so that they can be powered on/off by the control signals, as they will be turned off to save power when the SILBBPLL is injection-locked.

2.2 DCO structure and frequency tuning cirduits

2.2.1 *Overall structure*

Figure 4 shows the overall DCO structure with different frequency tuning circuit blocks. The DCO adopts a 4-stage differential structure and consumes much less power than the DCO with multiple tri-state buffers arrays [15–17]. The 6-bit OFDAC1, 5-bit OFDAC2 and 5-bit OFDAC3 are used for coarse frequency tuning, fine frequency tuning and ultra-fine frequency tuning. They convert the digital control words into a linear tuning voltage for DCO delay blocks and the varactors.

In a digital injection-locked PLL (IL-PLL), DCO frequency resolution is critical for reducing reference spurs. If the DCO frequency resolution is poor, a large phase shift will be derived from the injection locking point, which will cause large reference spurs. Therefore, the fine frequency tuning circuits block and ultra-fine frequency tuning circuits block are proposed to improve the DCO resolution. The OFDAC2 and OFDAC3 output the tuning voltages to the custom varactors to perform the fine tuning and ultra-

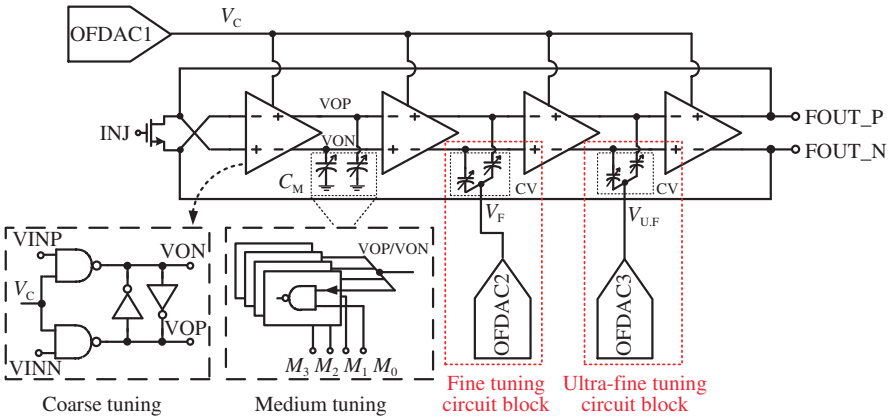


Figure 4 (Color online) DCO structure with frequency tuning circuits.

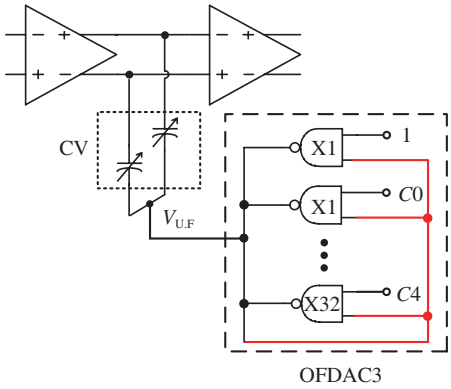


Figure 5 (Color online) Circuits of the ultra-fine tuning block.

fine tuning, respectively. The capacitance of the custom varactors can be much smaller than that of the standard cell. Therefore, the custom varactor based fine and ultra-fine frequency tuning can enhance the DCO resolution remarkably. They are designed as standard cells and added to the standard cells library. The capacitance of the custom varactor in the fine tuning circuit is larger than that in the ultra-fine tuning circuit. The varactors in the ultra-fine tuning circuits decide the least significant bit (LSB) of the DCO frequency resolution.

2.2.2 *Proposed ultra-fine frequency tuning circuits*

The main difference between the fine tuning and ultra-fine tuning is that the fine tuning block have larger tuning range and lower tuning resolution, while the ultra-fine tuning block decide the LSB of the DCO. So the following analysis will be focused on the ultra-fine frequency tuning only. Figure 5 shows the block diagram of the proposed ultra-fine tuning circuit. Two custom varactors are designed to perform the frequency tuning with the OFDAC3.

In a synthesized ADPLL, the inverter-based DAC (INV_DAC), the NAND-gate based DAC (NAND_DAC) [21–24], and the OFDAC can be adopted for supplying tuning voltage for the varactors. Figure 6(a) shows the block diagrams and Figure 6(b) shows the equivalent schematics of the INV_DAC, NAND_DAC and OFDAC. All the standard-cell based DACs operate based on the concept of voltage interpolation. Digital code D_N (N = 0, 1, 2, 3, 4) is used to control the on/off of the inverter or NAND gate. When D_N becomes larger, the output voltage becomes smaller.

Detailed theoretical analysis of the output voltage versus the digital control word of these three DACs is presented in Appendix A. Figure 7(a) presents the theoretical and simulated transfer curves of the DACs, respectively. Compared with the INV_DAC and the NAND_DAC, the OFDAC has following

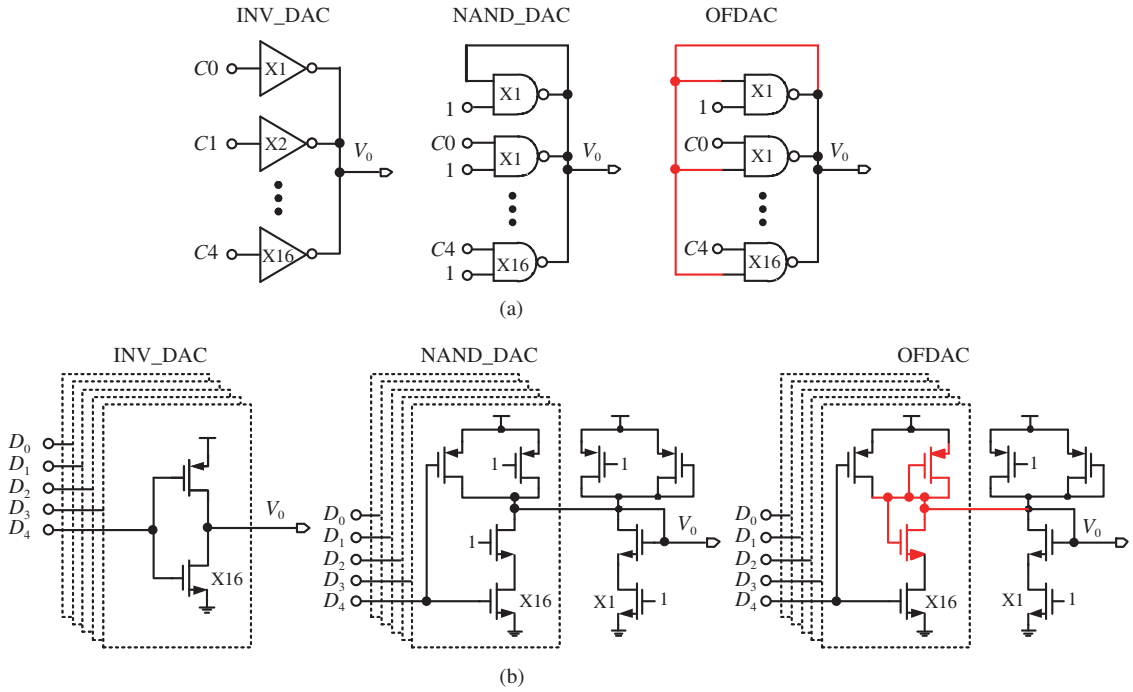


Figure 6 (Color online) (a) Block diagrams; (b) schematics of the VDAC, CDAC, and OFDAC.

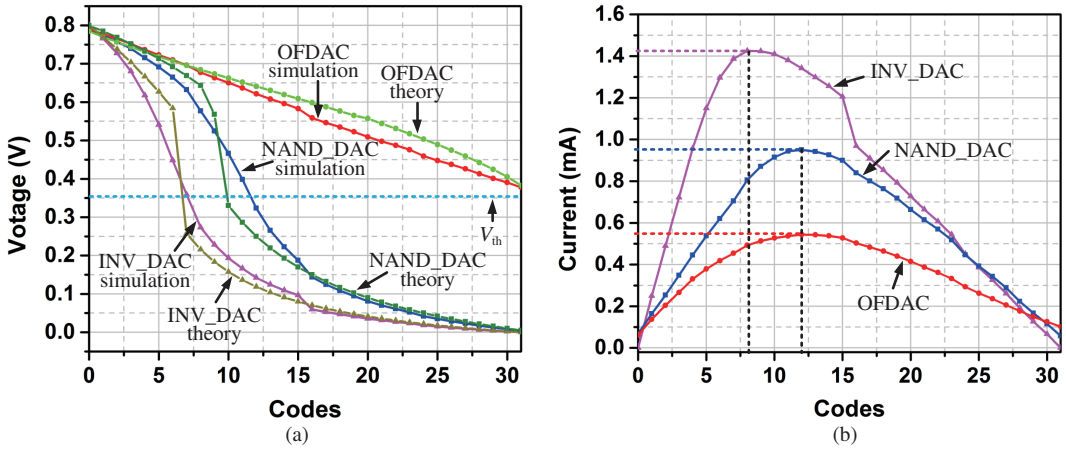


Figure 7 (Color online) (a) Theoretical and simulated transfer curves; (b) simulated power consumption of VDAC, CDAC, and OFDAC, respectively.

advantages. First, the OFDAC has a highly linear converted characteristic, which can improve the DCO frequency tuning linearity, thus reduce the spurs. Second, the OFDAC has a merit that the output voltage is always above the threshold voltage $V_{\rm th}$, which is critical for the coarse-tuning of the DCO, as will be explain later in the next sub-section. Third, as the simulated power consumption of the DACs shown in Figure 7(b), the OFDAC consumes about 70% and 45% less maximal-power, compared with the INV_DAC and the NAND_DAC, respectively. Therefore, the OFDAC has advantages of high linearity, low power and extensive usability.

Theoretically the varactor can be designed as small as possible to achieve extremely fine frequency tuning resolution. However, if the capacitance variance is too small, the unbalanced parasitic capacitors introduced by the APR, which modulates the DCO frequency, will become dominated in the frequency tuning. So the frequency tuning linearity will be severely deteriorated and the reference spurs become large. According to the analysis in [1], the minimum reference spurs that are at one reference frequency

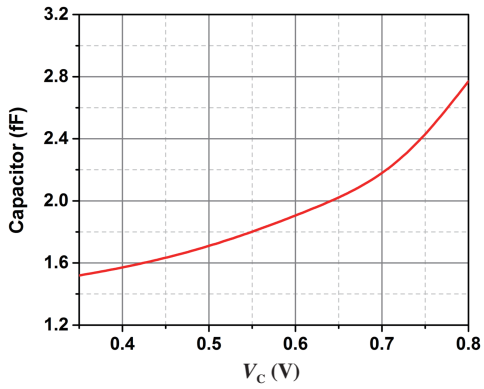


Figure 8 (Color online) Simulated capacitor variance against the control voltage.

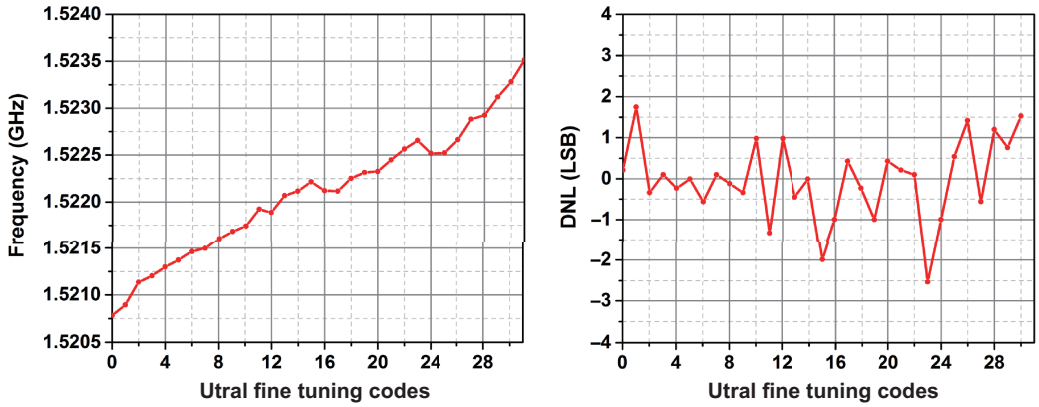


Figure 9 (Color online) Post-layout simulated (a) ultra-fine tuning versus codes (b) DNL.

offset due to DCO frequency resolution is given as

$$\beta_1 = a_1 \frac{\Delta f_{\rm res}}{f_{\rm m}}, \tag{1}$$

$$P(\text{dBc}) = 20 \log \left(\frac{\beta_1}{2} \right), \tag{2}$$

where $\Delta f_{\rm res}$ is the DCO frequency resolution, β_1 is the total reference spurs power at both sides of the oscillating frequency, and $(\beta_1/2)$ represents the reference spur power at each sides of the oscillating frequency. a_1 is the factor of the first harmonic in a Fourier decomposition, which is equal to $2/\pi$. $f_{\rm m}$ is the modulating frequency and it equals to one half of the reference clock (e.g. $f_{\rm REF}/2$) [1]. Based Eqs. (1) and (2), in order to achieve a reference spur level of less than -60 dBc, the DCO frequency resolution need to be smaller than 230 kHz/LSB with a reference clock of $f_{\rm REF} = 150$ MHz.

The simulated capacitance of the custom varactor in the ultra-fine tuning circuit block against the control voltage is shown in Figure 8. Its capacitance ranges from 1.5 to 2.8 fF when the control voltage $V_{\rm c}$ varies from 0.35 to 0.8 V. Combined with the 5-bit OFDAC3, the achieved unit variable capacitance is about 41 aF/LSB. It leads to a resolution about 90 kHz/LSB at 1.5 GHz, according to the simulation. Figure 9 shows the post-layout simulated tuning characteristic of the ultra-fine circuit block and the differential non-linearity (DNL). With the help of proposed ultra-fine tuning block, DCO frequency ranges from 1.5208 to 1.5235 GHz with promising linearity and an average resolution of 91 kHz/LSB. The DNL ranges from -2.5 to 1.8 LSB. The DNL is mainly influenced by the unbalanced parasitic introduced by APR. As shown in Figure 7(b), according to the simulation, the maximum current consumption of proposed ultra-fine tuning block (which is the current consumption of the OFDAC3, as the custom

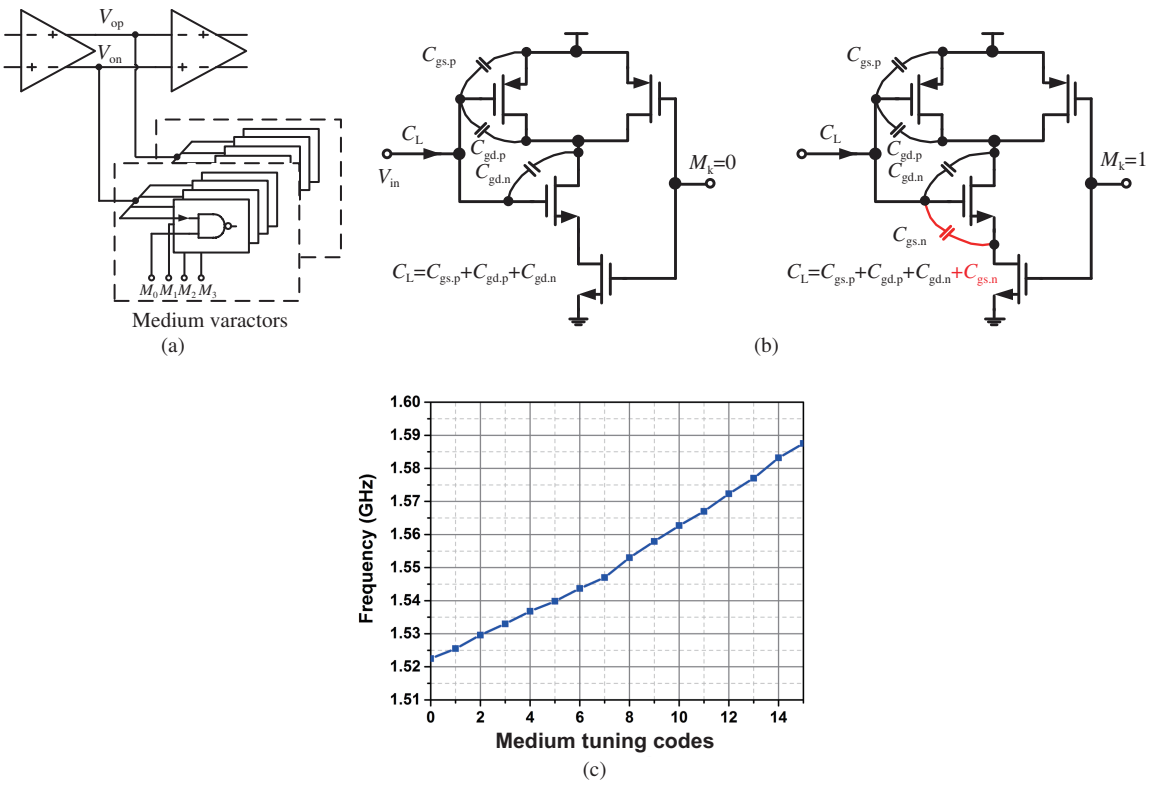


Figure 10 (Color online) (a) Detailed schematic of the medium tuning block; (b) tuning capacitor when $M_k = 0$ and $M_k = 1$, respectively; (c) medium frequency tuning characteristic of the DCO.

varactors do not consume currents) is less than 0.6 mA.

2.2.3 *Medium frequency tuning*

Generally, NAND-gate-based varactors can be adopted for DCO frequency tuning in a synthesized PLL [30]. The variable capacitance of the varactor is limited by the minimum size of the gates in the digital cells library. We adopt the NAND-gate-based varactors for DCO medium frequency tuning in this design. Figure 10(a) shows the detail schematic of the medium tuning block. 4 NAND-gate-based varactors with the same size are loaded to each delay stage of the DCO. As illustrated in Figure 10(b), the effective load capacitance of the delay cell in the DCO is different when the $M_k = 0$ and $M_k = 1$ ($k = 0, \ldots, 15$), respectively [30]. Therefore, frequency tuning can be implemented by setting the digital control words. Figure 10(c) shows the post-layout simulated tuning characteristic of medium tuning. The DCO frequency varies from 1.523 to 1.588 GHz, with a resolution as large as 4.3 MHz/LSB. According to Eqs. (1) and (2), this resolution can result in a reference spur about -35 dBc, which signifies the necessity of the fine and ultra-fine frequency tuning circuits for reducing reference spur.

2.2.4 *Coarse frequency tuning*

Given the advantages of the OFDAC, we further adopt the OFDAC to control a current starved oscillator as coarse tuning. As shown in Figure 4, the delay blocks in the DCO consist of two NAND gates and an inverters-based latch. As shown in Figure 11(a), the NAND gate in the delay blocks can be equivalent of an inverter with a voltage control current source (VCCS). The current of the DCO can be controlled by a tuning voltage V_C, which is supplied by the OFDAC in this design. Therefore, coarse frequency tuning of the DCO can be implemented using the OFDAC.

The tuning voltage V_C of the DCO has to be designed carefully, in order to achieve wide frequency tuning range of the DCO and to ensure the oscillation of the DCO. As analyzed in the previous subsection, the OFDAC has merits of high linearity and low power, so it is very suitable to adopt the OFDAC

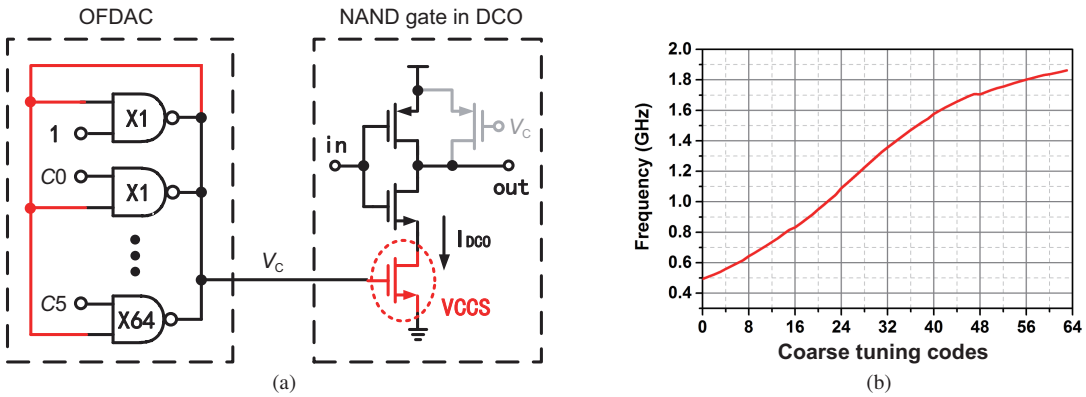


Figure 11 (Color online) (a) Block diagrams of coarse frequency tuning using OFDAC; (b) coarse frequency tuning characteristic of the DCO.

to supply linear tuning voltage for the DCO. Besides, compared with the INV_DAC and the NAND_DAC, the OFDAC has another merit that the output voltage is always above the threshold voltage $V_{\rm th}$, so it can ensure the oscillation and suitable coarse frequency tuning resolution of the DCO. Figure 11(b) presents the post layout coarse frequency tuning curve of the DCO using the OFDAC. With the help of the OFDAC, the DCO achieve a wide tuning range from 0.5 to 1.9 GHz.

2.3 Injection locking

Injection locking has been proven to be a promising technique to achieve low jitter performance in a PLL [31–35]. Therefore, it is adopted to reduce the phase noise by eliminating the DCO jitter accumulation at every reference cycle. The injection timing needs to be carefully calibrated in order to achieve fine jitter clearance effect and obviate from causing large reference spurs. In this design, we adopt a PG to conduct the pulse injection locking. A standard cell based DCDL which is based on the NAND-gate varactors is adopted to adjust the injection timing between the injection pulse and DCO output. Figure 12(a) shows the schematic of PG and DCDL. The digital control varactors in the DCDL are based on the NAND gates. The delay time of the injection pulse in relative to the reference clock (REF) is manually selected by the delay control words P[5:0]. Figure 12(b) shows the waveforms relationship of the REF, injection pulse (INJ), and DCO output signal (FOUT) in ideal case. We set the INJ to be aligned with the rising edge of REF. Ideally, when PLL2 is locked, REF will be aligned with the crossing point of FOUT. So the INJ will also be aligned to the crossing point of FOUT and be injected to the DCO for phase realignment. Thus, the injection locking is conducted [29]. However, in practice, due to the delay from the REF to the BBPD input, the intrinsic delay inside the BBPD, and the PVT variations, the PLL2 might lock the DCO but there still a static phase error θ exist between the REF and FOUT, as shown in Figure 12(c). Thus, by setting the delay time of the DCDL, the INJ can be calibrated to be aligned with FOUT for injection locking.

3 Implementation and measurement results

The SILBBPLL is implemented in a 65 nm CMOS process. All circuits are described with HDL and APR using standard digital design flow. Core area of the SILBBPLL is 0.008 mm^2. Die photograph and layout of the SILBBPLL are shown in Figure 13. Measured operating frequency of SILBBPLL ranges from 0.45 to 1.8 GHz with a 0.8-V supply.

Figure 14 shows the measured phase noise of the SILBBPLL at 0.9, 1.5 and 1.8 GHz, respectively. The frequency of the reference clock is 150 MHz. As shown in the figure, the phase noise of the SILBBPLL is improved by the injection-locking. When operating at 1.8 GHz, the RMS jitter with injection-locking integrated from 10 kHz to 100 MHz is 1.1 ps. The power consumption excluding the output buffer is 1.5 mW.

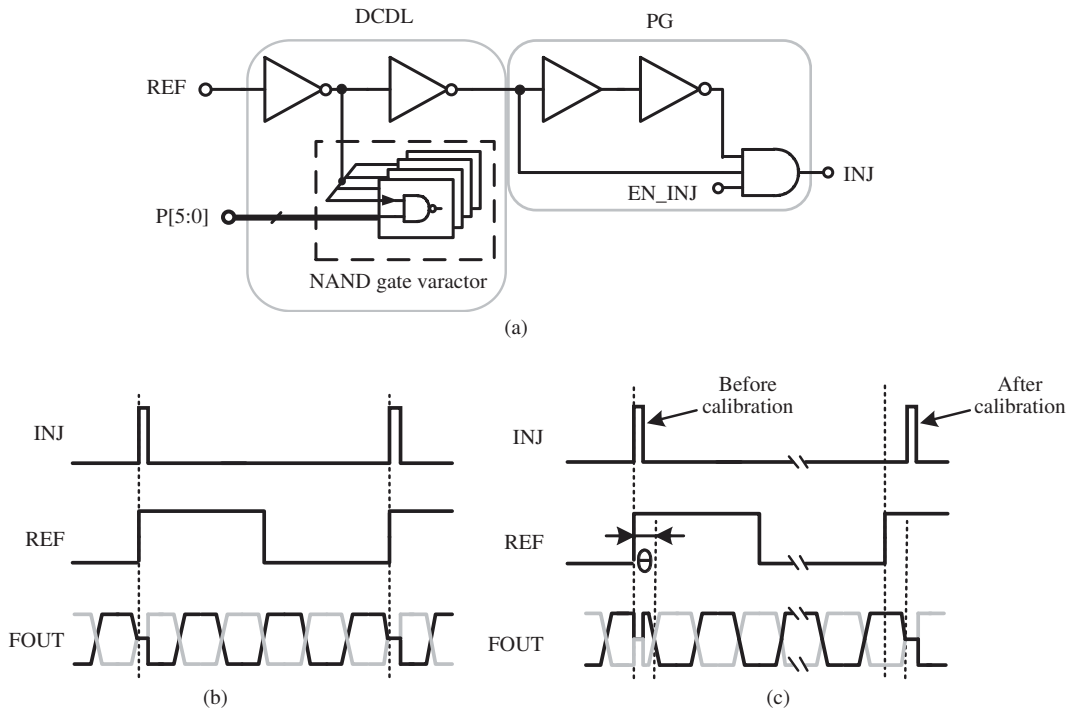


Figure 12 (a) Schematic of PG and DCDL; (b) waveforms relationship of REF, INJ and FOUT in ideal case; (c) waveforms relationship with static error exist between REF and FOUT.

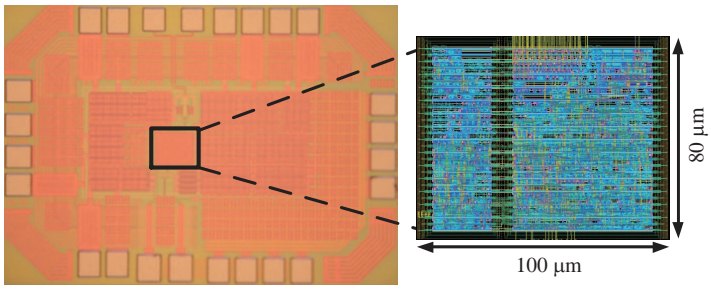


Figure 13 (Color online) Die photograph and the layout of the SILBBPLL.

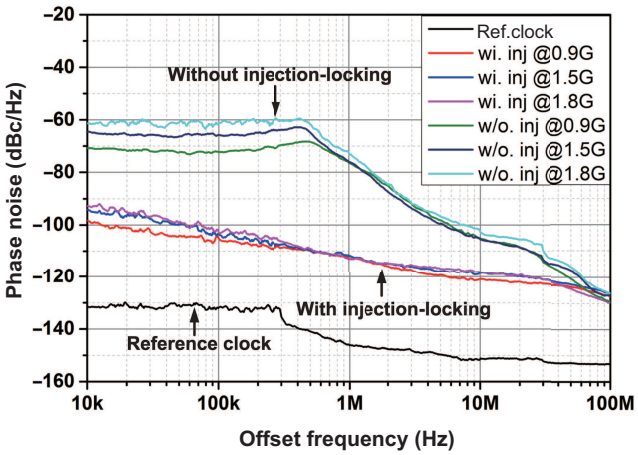


Figure 14 (Color online) Measured phase noise of the SILBBPLL at 0.9, 1.5 and 1.8 GHz, respectively.

Figure 15 shows the measured spectrum of the output signal without and with injection locking at 1.8 GHz. Without injection locking, the reference spur at 150 MHz is −55.8 dBc. With injection locking,

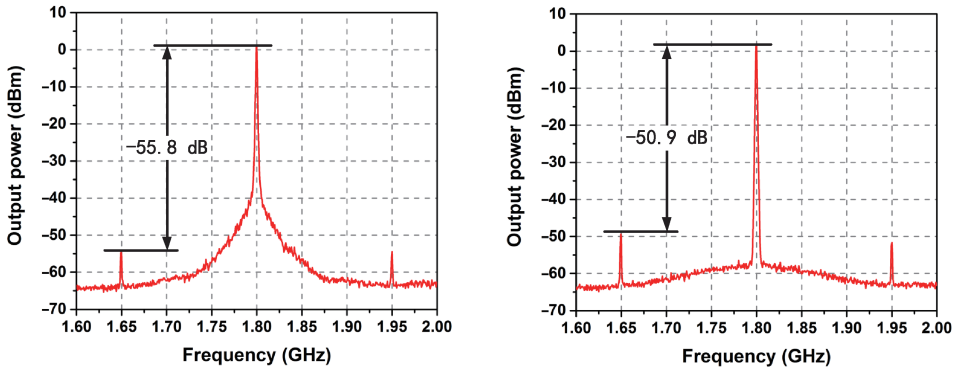


Figure 15 (Color online) Measured spectrum of the output signal at 1.8 GHz (a) without injection locking; (b) with injection locking.

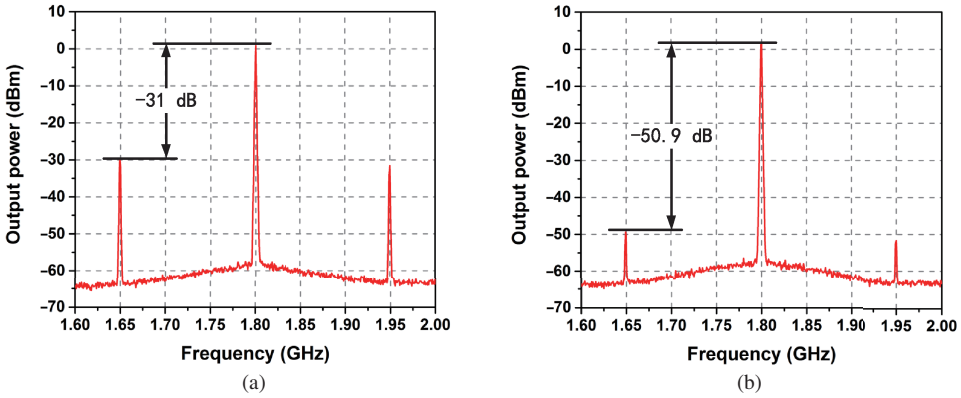


Figure 16 (Color online) Measured spectrum of the output signal (a) without proposed frequency tuning circuits, and (b) with the proposed frequency tuning circuits.

the reference spur at 150 MHz is −50.9 dBc. Because of the mismatch issues and interferences in the synthesized circuits, and the DNL of the tuning blocks, the reference spur without injection locking is higher than the theoretical results. Due to the limited resolution of the DCDL in this design, there is static error remained between the INJ and FOUT (Figure 12) after the calibration. So the reference spur with injection locking is higher than that without injection locking.

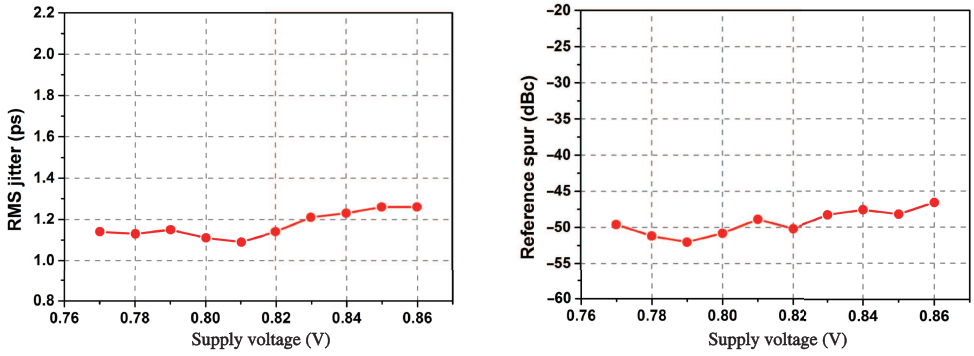
Figure 16 shows the measured spectrum of the output signal without and with the proposed fine and ultra-fine frequency tuning circuits when the SIBBPLL is injection locked. As shown in the figure, without the proposed frequency tuning circuits the reference spur is −31 dBc, whereas with the proposed frequency tuning circuits, the reference spur is −50.9 dBc. The reference spur is reduced by 19.9 dB, which proves the effectiveness of the fine and ultra-fine frequency tuning circuits for improving the reference spur.

Figure 17(a) shows the measured RMS jitter at 1.8 GHz versus supply voltage and Figure 17(b) shows the measured spur level against supply voltage. The jitter variances are less than 0.3 ps and the spur level are less than −45 dBc, when the supply voltage varies from 0.77 to 0.86 V. Therefore, with the injection locking, the SILBBPLL is robust to the supply voltage variances.

Table 1 summarizes the performance of this work and the previous synthesized ADPLLs. A figure-of-merit (FoM) considering the trade-off of the jitter and power performances is adopted to fairly compare the performance of the PLLs. The FoM is defined as follows [36]:

$$\mathrm{FoM} = 20\log\left(\frac{\sigma_{\mathrm{rms}}}{1\ \mathrm{s}}\right) + 10\log\left(\frac{P}{1\ \mathrm{mW}}\right), \tag{3}$$

where σ_{rms} is the RMS jitter, P is the power consumption of the PLL. The SILBBPLL achieves one of the



(a) (b)

Figure 17 (Color online) (a) Measured RMS jitter; (b) measured spur level at 1.8 GHz versus supply voltage variations.

Table 1 Performance summary and comparison

	This work	[18]	[22]	[23]	[19]	[15]	[16]
Technology (nm)	65	65	65	28	65	65	65
Frequency (GHz)	0.45–1.8	2	0.39–1.41	1.6	2.8–3.2	1.5–2.7	0.403
Ref. clock (MHz)	150	64	40–350	400	150	10	40.3
Power (mW)	1.5	10.8	0.78	1.4	4.6	13.7	2.1
Frequency (GHz)	1.8	2	0.9	1.6	3	2.5	0.4
Area (mm^2)	0.008	0.047	0.0066	0.004	0.12	0.042	0.1
RMS jitter (ps)	1.1	3.15	1.7	1.5	0.14	3.2	13.3
(range)	[10 k, 100 M]	[10 k, 100 M]	[10 k, 40 M]	[1 k, 10 M]	[10 k, 40 M]	–	–
Ref. supr (dBc)	−50.9	–	−42	−39	−47	–	–
FoM (dB)	−237.4	−219.7	−236.5	−235.0	−250.3	−218.6	−214.3

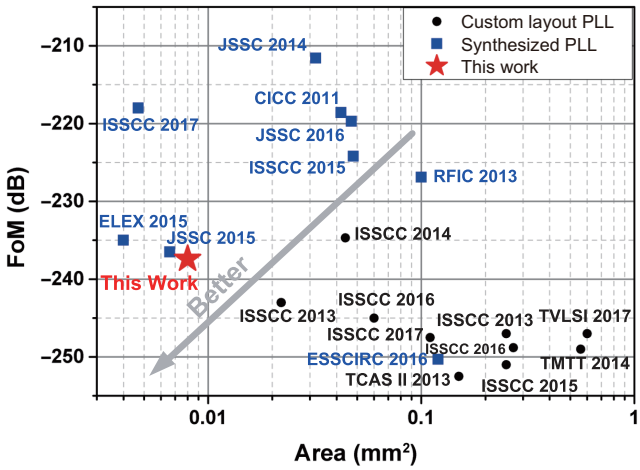


Figure 18 (Color online) Performance of this work with the recently published synthesized PLLs and custom layout injection-locked PLLs.

best FoM and the lowest reference spur level, compared with previous synthesized ADPLLs. Figure 18 compares the performance of this work with the recently published synthesized ADPLLs and customized layout injection-locked PLLs.

4 Conclusion

A SILBBPLL with high DCO resolution was proposed and verified in 65 nm CMOS process. All circuits of the SILBBPLL were described with HDL and APR using standard digital circuit design flow. As DCO

frequency resolution is critical for reducing the reference spur in a digital IL-PLL, we proposed novel frequency tuning circuits to increase the DCO frequency resolution so that the reference spur is reduced. Measured results showed that when operating at 1.8 GHz, the SILBBPLL achieved RMS jitter of 1.1 ps, and the power consumption is 1.5 mW. The proposed SILBBPLL achieved an FoM of −237.4 dB. The reference spur is −50.9 dBc.

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Appendix A

Figure A1 presents the detail schematic of the OFDAC. $I_{\rm n(}_{j}_{\rm)}$ ($j = 0, N-1$) is the current of the feedback NMOS (F_NMOS) and controlled NMOS (C_NMOS) in the NAND gate, $I_{\rm p(}_{j}_{\rm)}$ is current of the feedback PMOS (F_PMOS), and $i_{\rm p(}_{j}_{\rm)}$ is the current of the controlled PMOS (C_PMOS). The currents that through the transistors of the $j_{\rm th}$ NAND gate are calculated as follows:

$$I_{\rm n(}_{j}_{\rm)} = I_{\rm n(0)} \cdot 2^j, \tag{A1}$$

$$I_{\rm p(}_{j}_{\rm)} = I_{\rm p(0)} \cdot 2^j, \tag{A2}$$

$$i_{\rm p(}_{j}_{\rm)} = i_{\rm p(0)} \cdot 2^j, \tag{A3}$$

where $I_{\rm n(0)}$ is the current of the F_NMOS of the minimal NAND gate, $I_{\rm p(0)}$ and $i_{\rm p(0)}$ are the current of the F_PMOS and C_PMOS of the minimal NAND gate, respectively. 2^j represents the current ratio between the $j_{\rm th}$ NAND gate and the minimal NAND gate. Assuming the control word of the OFDAC is equal to m, which is expressed as follows:

$$m = 2^{N-1} \cdot D_{N-1} + \cdots + 2^0 \cdot D_0. \tag{A4}$$

Then the total current that through all the F_NMOS, the C_PMOS and the F_PMOS of the OFDAC is

$$I_{\rm n\_all} = I_{\rm n(0)} \cdot 1 + I_{\rm n(0)} \cdot D_0 + \cdots + I_{\rm n} \cdot D_{N-1} = (m+1) \cdot I_{\rm n(0)}, \tag{A5}$$

$$I_{\rm p\_all} = I_{\rm p(0)} + I_{\rm n(0)} + \cdots + I_{p(N-1)} = I_{\rm n(0)}(1 + 1 + \cdots + 2^{N-1}) = 2^N \cdot I_{\rm p(0)}, \tag{A6}$$

$$i_{\rm p\_all} = i_{\rm p(0)} \cdot \overline{D_0} + \cdots + i_{p(N-1)} \cdot \overline{D_{N-1}} = (2^N - 1 - m) \cdot i_{\rm p(0)}. \tag{A7}$$

According to the first Kirchhoff's Law,

$$I_{\rm n\_all} = i_{\rm p\_all} + I_{\rm p\_all}. \tag{A8}$$

We use $V_{\rm O}$ as the output voltage of the OFDAC. As the $V_{\rm O}$ varies, the transistors in the NAND gates work at different regions. We start from when the $V_{\rm O} < {\rm VDD} - V_{\rm th}$. In this case, all the F_PMOSs are in saturation region despite of the control code, and the current through F_PMOSs is $I_{\rm p\_all}$. According to (A7), at least the same current will run through the F_NMOS. As the F_NMOS is diode-connected, so the F_NMOS will be in saturation region. Therefore, the following equality can be satisfied for any input code:

$$V_{\rm O} > V_{\rm th}. \tag{A9}$$

When $V_{\rm O} > V_{\rm th}$, for the C_PMOS, if it is switched on by $D_{j-1} = 0$ ($j = 1, N-1$), then the following inequality can be derived:

$$|V_{\rm gs\_C\_PMOS} - V_{\rm th}| = {\rm VDD} - 0 - V_{\rm th} > {\rm VDD} - V_{\rm O}, \tag{A10}$$

$$|V_{\rm ds\_C\_PMOS}| = {\rm VDD} - V_{\rm O}, \tag{A11}$$

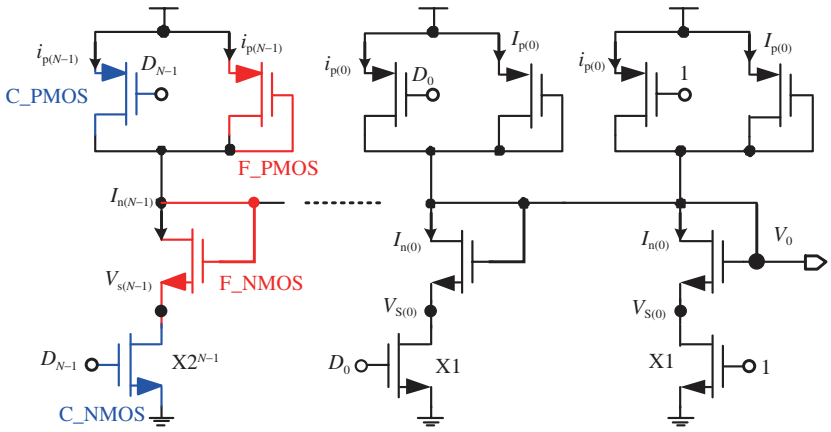

Figure A1 (Color online) Detailed schematic and the currents in each transistors of the OFDAC.

where VDD is the source supply voltage, $V_{\rm gs\_C\_PMOS}$ is the gate-source voltage of the C_PMOS, $V_{\rm ds\_C\_PMOS}$ is the drain-source voltage of the C_PMOS. From (A10) and (A11) we have

$$|V_{\rm gs\_C\_PMOS} - V_{\rm th}| > |V_{\rm ds\_C\_PMOS}|. \tag{A12}$$

Therefore, from (A12) it can be concluded that the C_PMOS will always be in a transistor region if it is switched on by the digital control word.

As for the C_NMOS, if it is switched on by $D_{j-1} = 1$, then the following can be derived:

$$|V_{\rm gs\_C\_NMOS} - V_{\rm thn}| = {\rm VDD} - V_{\rm th}, \tag{A13}$$

$$|V_{\rm ds\_C\_NMOS}| = V_{\rm out} - V_{\rm gs\_F\_NMOS} < {\rm VDD} - V_{\rm gs\_F\_NMOS}, \tag{A14}$$

$$V_{\rm gs\_F\_NMOS} > V_{\rm th}, \tag{A15}$$

where $V_{\rm gs\_C\_NMOS}$ is the gate-source voltage of the C_NMOS, $V_{\rm ds\_C\_NMOS}$ is the drain-source voltage of the C_NMOS and $V_{\rm gs\_F\_NMOS}$ is the gate-source voltage of the F_NMOS. From (A13)–(A15) we have

$$|V_{\rm gs\_C\_NMOS} - V_{\rm thn}| = V_{\rm ds\_C\_NMOS}. \tag{A16}$$

From (A16) it can be conclude that the C_NMOS will always be in a transistor region if it is switched on by the digital control word.

So there are 2 cases for the calculation of $V_{\rm O}$ in the OFDAC.

Case 1. If $V_{\rm th} < V_{\rm O} < {\rm VDD} - V_{\rm th}$, both the F_PMOS and the F_NMOS are in saturation region, and both the C_PMOS and C_NMOS are in the transistor region. Thus the $I_{\rm n(0)}$, $I_{\rm p(0)}$ and $i_{\rm p(0)}$ can be expressed as follows:

$$I_{\rm n(0)} = \frac{1}{2}K_{\rm n}\left(\frac{W_{\rm n(0)}}{L_{\rm n(0)}}\right)(V_{\rm O} - V_{\rm s0} - V_{\rm thn})^2, \tag{A17}$$

$$I_{\rm p(0)} = \frac{1}{2}K_{\rm p}\left(\frac{W_{\rm p(0)}}{L_{\rm p(0)}}\right)({\rm VDD} - V_{\rm O} - V_{\rm thp})^2, \tag{A18}$$

$$i_{\rm p(0)} = K_{\rm p}\left(\frac{W_{\rm p(0)}}{L_{\rm p(0)}}\right)({\rm VDD} - V_{\rm thp})({\rm VDD} - V_{\rm O}), \tag{A19}$$

where $K_{\rm n} = \mu_{\rm n}c_{\rm oxn}$ and $K_{\rm p} = \mu_{\rm p}c_{\rm oxp}$, $\mu_{\rm n}$ and $\mu_{\rm p}$ carrier mobility of the NMOS and PMOS, $c_{\rm oxn}$ and $c_{\rm oxp}$ are the gate oxide capacitor of the transistor. $W_{\rm n(0)}$ and $L_{\rm n(0)}$ are the width and length of NMOS of the minimal NAND gate. $W_{\rm p(0)}$ and $L_{\rm p(0)}$ are width and length of PMOS of the minimal NAND gate. For the NMOS and PMOS of the NAND gate in this design, the following equality is satisfied:

$$K_{\rm n} = 2K_{\rm p}. \tag{A20}$$

As the C_NMOS is in transistor region and it is cascaded with the F_NMOS, which is in the saturation region, so if any C_NMOS is switched on by the digital control word, $V_{\rm s(j-1)}$ will be very small. For the simplicity of the calculation, it can be equal to 0, i.e., $V_{\rm s(j-1)} = 0$. Therefore, (A17) can be re-written as follows:

$$I_{\rm n(0)} = \frac{1}{2}K_{\rm n}\left(\frac{W_{\rm n(0)}}{L_{\rm n(0)}}\right)(V_{\rm O} - V_{\rm thn})^2. \tag{A21}$$

For the NAND gate we used in this design, the width of the PMOS and NMOS is equal, that is

$$\frac{W_{\rm n(0)}}{L_{\rm n(0)}} = \frac{W_{\rm p(0)}}{L_{\rm p(0)}}. \tag{A22}$$

From (A4)–(A7) and (A17)–(A22), the $V_{\rm O}$ can be derived as follows:

$$V_{\rm O}=\frac{(a_1{\rm VDD}-a_2V_{\rm th})-\sqrt{(a_1{\rm VDD}-a_2V_{\rm th})^2-4a_0c}}{2a_0}, \tag{A23}$$

where

$$a_0=2^N-2m-2\ \ \&\ \ m\neq 2^{N-1}-1, \tag{A24}$$

$$a_1=2^{N+2}-2m-2, \tag{A25}$$

$$a_1=2^{N+2}-2m+2, \tag{A26}$$

$$c=(a_0+2^{N+1}){\rm VDD}^2-a_1{\rm VDD}\cdot V_{\rm th}+a_0V_{\rm th}^2, \tag{A27}$$

and

$$V_{\rm O}=\frac{(2{\rm VDD}-3V_{\rm th}){\rm VDD}}{3{\rm VDD}-5V_{\rm th}},\quad m=2^{N-1}-1. \tag{A28}$$

Case 2. If ${\rm VDD}-V_{\rm th}<V_{\rm O}<{\rm VDD}$, the F_PMOS is in sub-threshold region, the F_NMOS is in saturation region, and both the C_PMOS and C_NMOS are in the transistor region. Thus the current of the F_PMOS can be equal to about 0, which is

$$I_{\rm p(0)}\approx 0. \tag{A29}$$

And the current of F_NMOS $I_{\rm n(0)}$ and the C_PMOS $i_{\rm p(0)}$ can be expressed as follows:

$$I_{\rm n(0)}=\frac{1}{2}K_{\rm n}\left(\frac{W_{\rm n(0)}}{L_{\rm n(0)}}\right)(V_{\rm O}-V_{\rm thn})^2, \tag{A30}$$

$$i_{\rm p(0)}=K_{\rm p}\left(\frac{W_{\rm p(0)}}{L_{\rm n(0)}}\right)({\rm VDD}-V_{\rm thp})({\rm VDD}-V_{\rm O}). \tag{A31}$$

From (A4)–(A7), (A18) and (A29)–(A31), the $V_{\rm O}$ can be derived as follows:

$$V_{\rm O}=\frac{({\rm VDD}+V_{\rm th})}{2}-\frac{({\rm VDD}-V_{\rm th})(2^N-\sqrt{2^{2N}+2^{N+1}+m(2^{N+1}-3m-6)-3)})}{2(m+1)}. \tag{A32}$$

Following the same analysis, the output voltage of the INV_DAC and NAND_DAC can also be derived as follows:

$$V_{\rm O\_INV\_DAC}=\begin{cases}\dfrac{(2^N-1-3m){\rm VDD}+2nV_{\rm th}}{2^N-1-m}, & {\rm VDD}-V_{\rm th}<V_{\rm O\_INV\_DAC};\\ \dfrac{(2^N-1-m){\rm VDD}}{2^N-1+3m}, & V_{\rm th}<V_{\rm O\_INV\_DAC}\leqslant {\rm VDD}-V_{\rm th};\\ \dfrac{(2^N-m)({\rm VDD}-V_{\rm th})}{3m}, & V_{\rm O\_INV\_DAC}\leqslant V_{\rm th},\end{cases} \tag{A33}$$

$$V_{\rm O\_NAND\_DAC}=\begin{cases}\dfrac{b_1^2-\sqrt{b_1^2-4c_1}}{2}, & {\rm VDD}-V_{\rm th}<V_{\rm O\_NAND\_DAC};\\ \dfrac{b_2^2-\sqrt{b_2^2-4c_2}}{6}, & V_{\rm th}<V_{\rm O\_NAND\_DAC}\leqslant {\rm VDD}-V_{\rm th};\\ \dfrac{(2^N-m)({\rm VDD}-V_{\rm th})}{6m}, & V_{\rm O\_NAND\_DAC}\leqslant V_{\rm th},\end{cases} \tag{A34}$$

where

$$b_1=(2^{N+2}-4m-4)({\rm VDD}-V_{\rm th})+4V_{\rm th}, \tag{A35}$$

$$c_1=(2^{N+2}-8m-4)({\rm VDD}^2-{\rm VDD}\cdot V_{\rm th})+4m{\rm VDD}\cdot V_{\rm th}+(4-4m)V_{\rm th}^2, \tag{A36}$$

$$b_2=2^{N+2}({\rm VDD}-V_{\rm th})+4V_{\rm th}, \tag{A37}$$

$$c_2=(2^{N+2}-4m)({\rm VDD}^2-{\rm VDD}\cdot V_{\rm th})-2{\rm VDD}^2+6V_{\rm th}^2, \tag{A38}$$

where $V_{\rm O\_INV\_DAC}$ and $V_{\rm O\_NAND\_DAC}$ are the output voltage of the INV_DAC and NAND_DAC, respectively. The theoretical and simulated output voltage versus against the control code is presented in Figure 7(a). The source supply is 0.8 V, the OFDAC input control word is 5*b* and the threshold voltage is about 0.35 V in this design. The deviations between the theoretical and simulated output voltage are mainly caused by the body-effect of the transistor and the weak current of the transistor in the sub-threshold region, which is assumed to be 0 in the theoretical calculation.