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Short-channel effects on the static noise margin of 6T SRAM composed of 2D semiconductor MOSFETs

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Abstract This paper investigates the influence of the short-channel effects (SCEs) on the static noise margin (SNM) of 6T (6 transistors) SRAM composed of 2D MOSFETs. An analytical all-region I-V model for short-channel complementary 2D MOSFETs has been developed, and a simulation model has been built to calculate SNM with the consideration of SCEs and velocity saturation. The results show that there exists an optimal value of channel length ($L_{\rm opt}$) where SNM reaches a maximum, and $L_{\rm opt}$ is approximately three times the scale length. In the region where $L>L_{\rm opt}$, SNM increases slightly as L decreases because of velocity saturation, while in the region where $L<L_{\rm opt}$, SNM decreases rapidly as L decreases as the SCEs are dominant. The worst case of SNM reduction due to the threshold voltage (V_T) fluctuation is investigated, and the maximum V_T tolerance is studied as a function of L. In an SRAM with a scale length of 5 nm, as L decreases from 15 nm to 5 nm, SNM decreases from 155 mV to 98 mV, and the maximum V_T tolerance decreases from 126 mV to 105 mV.

Keywords 2D semiconductor, model, SNM, SCEs, SRAM

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1 Introduction

Two-dimensional (2D) semiconductor materials such as transition metal dichalcogenides (TMD) can achieve a uniform atomic-scale thickness channel with a dangling bond-free surface, making them a promising candidate in the sub-7 nm technology [1–5]. A drift and diffusion long-channel I-V model for 2D MOSFETs has been developed [6]. Short-channel effects (SCEs) [7,8] and velocity saturation [9] are considered and modeled for an N-type 2D MOSFET in [10]. A simulation model based on an analytical long-channel I-V model has been built to investigate the effects on the static noise margin (SNM) of contact resistance and inefficient channel doping [11]. As device dimensions are scaled down, the operation voltage and threshold voltage decrease, leading to the decrease in SNM. An adequate SNM is desired to ensure the reliability and stability of 6T (6 transistors) SRAM [12,13]. To investigate the influence of SCEs on the SNM of 6T SRAM composed of 2D MOSFETs, this work investigates analytical all-region I-V model for short-channel complementary 2D MOSFETs and simulation model to calculate SNM with the consideration of SCEs and velocity saturation.

In this paper, we present the I-V current model for P-type 2D MOSFETs, and build the unified current form for both N-type and P-type 2D MOSFETs. The current model includes both SCEs and velocity saturation. Based on the analytical all-region I-V model, the simulation model to calculate the

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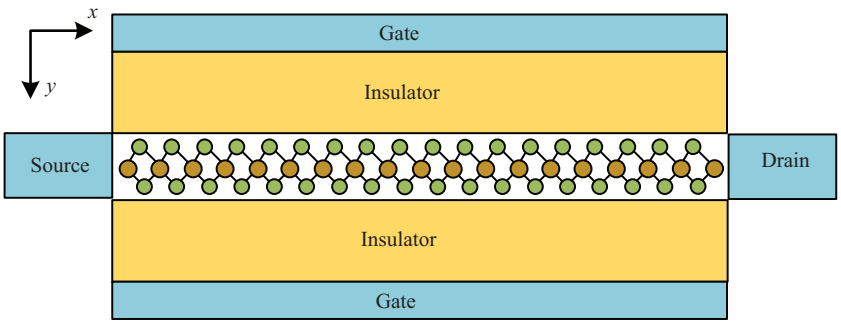

Figure 1 (Color online) Structure of 2D DG MOSFET.

output-input curve for an inverter with an access MOSFET is developed, and SNM can be calculated from the output-input curves of the two cross-coupled inverters in a 6T SRAM. The dependency of SNM on channel length is investigated. The worst case of SNM reduction caused by threshold voltage (V_T) fluctuation is investigated by exactly mismatching the two inverters, and the relationship between maximum V_T tolerance and L is established.

2 All-region *I*-*V* model for 2D complementary MOSFETs

The basic structure of 2D DG MOSFET is shown in Figure 1. The gates are located at the bottom and top of 2D material channel. The same voltage is applied to both the bottom and top gates. The complementary all-region I-V model is composed of a P-type all-region model and an N-type all-region model. These two models are unified to constitute a combined complementary model.

The all-region I-V model is composed of two parts: a short-channel model to describe the subthreshold current, and a velocity saturation model to describe the ON-current. The final all-region I-V model is achieved by splicing these two models together at the threshold voltage.

First, the short-channel subthreshold current model is obtained by analytically solving the 2D potential in the subthreshold region. The source Fermi level is assumed to be located at the valence-band edge of the source serving as the zero-potential reference.

For a 2D semiconductor channel, the inversion charge density can be expressed in terms of the 2D density of states (DOS) and Fermi statistics. The DOS for holes in 2D semiconductors is obtained as follows:

$$P_{\mathrm{DOS}} = \frac{2\pi g_{\mathrm{v}} g_{\mathrm{s}} m_{\mathrm{h}}^*}{h^2}, \tag{1}$$

where g_{v} and g_{s} are the valley degeneracy and spin degeneracy, respectively, and m_{h}^* is the effective hole mass.

By taking the integral of 2D DOS and Fermi-Dirac distribution function, the inversion charge density for holes can be expressed as follows:

$$Q_i(x) = \frac{2\pi g_{\mathrm{v}} g_{\mathrm{s}} m_{\mathrm{h}}^* kT}{h^2} \ln\left[1 + \mathrm{e}^{q[V(x)-\psi(x)]/kT}\right], \tag{2}$$

where $V(x)$ is the quasi-Fermi potential at position x; $V(0) = 0$ at the source, and $V(L) = V_{\mathrm{ds}}$ at the drain; $\psi(x)$ is the potential in the channel which can be solved using Poisson's equation.

Because the mobile charge can be omitted in the subthreshold region, the Poisson's equation can be written as follows:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = 0, \tag{3}$$

where x is the direction along the channel and y is the direction perpendicular to the channel. The origin of coordinate is the source side of channel.

The boundary conditions of Poisson's equation are as follows:

$$\begin{cases} \psi(x,-t_i) = V_{\rm gs} - \Delta\phi, & 0 \leqslant x \leqslant L, \\ \psi(x,t_i) = V_{\rm gs} - \Delta\phi, & 0 \leqslant x \leqslant L, \\ \psi(0,0) = 0, \\ \psi(L,0) = V_{\rm ds}. \end{cases} \tag{4}$$

The four boundary conditions correspond to the potential on the top, bottom, source, and drain of device. The potential of insulator gap region between gates and source/drain has a linear relationship with y. For example, $\psi(0,y) = y(V_{\rm gs} - \Delta\Phi)/t_i$ for $0<y<t_i$, where t_i is the thickness of insulator. The other three gaps have similar expressions.

As the thickness of a 2D material channel approaches zero, the potential of channel is a function of x, and the lowest-order scale length λ is equals to the thickness of insulator $2t_i$. By solving the Poisson's equation, the potential of a channel can be expressed as follows:

$$\psi(x) = -(V_{\rm gs} - \Delta\phi)\frac{\sinh[\pi(L-x)/2t_i]}{\sinh(\pi L/2t_i)} + (V_{\rm gs} - \Delta\phi) + (V_{\rm ds} - V_{\rm gs} + \Delta\phi)\frac{\sinh(\pi x/2t_i)}{\sinh(\pi L/2t_i)}. \tag{5}$$

Using the drift-diffusion transport model and current continuity equation, the subthreshold drain current of P-type 2D DG MOSFET can be obtained as follows:

$$I_{\rm ds} = \mu W \frac{2\pi g_{\rm v} g_{\rm s} m_{\rm h}^* (kT)^2}{h^2} \frac{{\rm e}^{qV_{\rm ds}/kT} - 1}{\int_0^L {\rm e}^{q\psi(x)/kT}{\rm d}x}. \tag{6}$$

Second, for a long-channel on-state current model [14], under the conditions for charge and potential in the direction perpendicular to the 2D film:

$$V_{\rm gs} - \Delta\Phi - \psi(x) = \frac{Q_i(x)/2}{C_{\rm OX}}. \tag{7}$$

By substituting (2) into (7), V can be solved in terms of ψ. The relationship between V and ψ can be written as follows:

$$V = \psi + \frac{kT}{q}\ln\left\{-\exp\left[\frac{h^2 C_{\rm OX}}{g_{\rm v} g_{\rm s}\pi q m_{\rm h}^* kT}(V_{\rm gs} - \Delta\Phi - \psi)\right] - 1\right\}. \tag{8}$$

Velocity saturation is implemented in the model using a field-dependent mobility in the current expression:

$$I_{\rm ds} = W Q_i \frac{\mu_0}{1 - (\mu_0/v_{\rm sat})({\rm d}\psi/{\rm d}x)}\frac{{\rm d}V}{{\rm d}x}, \tag{9}$$

where μ_0 is the low-field mobility and $v_{\rm sat}$ is the saturation velocity. By converting ${\rm d}V$ to ${\rm d}\psi$ and solving for ${\rm d}\psi/{\rm d}x$, the current expression is integrated as

$$I_{\rm ds} = \frac{\mu_0 W}{L - (\mu_0/v_{\rm sat})(\psi_{\rm d} - \psi_{\rm s})}\int_{\psi_{\rm s}}^{\psi_{\rm d}} Q_i \frac{{\rm d}V}{{\rm d}\psi}{\rm d}\psi. \tag{10}$$

In this expression, if $I_{\rm ds}$ is considered as a function of $\psi_{\rm d}$, $I_{\rm ds}$ first increases, reaches a peak value, and then decreases with $\psi_{\rm d}$. The peak value $I_{\rm ds}$ occurs at $\psi_{\rm d} = \psi_m$, and the $I_{\rm ds}$ will saturate beyond ψ_m point. The ψ_m is set as the upper limit of $\psi_{\rm d}$. If $\psi_{\rm d}$ is smaller than ψ_m, the current expression uses the actual $\psi_{\rm d}$, and if $\psi_{\rm d}$ is larger than ψ_m, $\psi_{\rm d}$ in (10) should be replaced with ψ_m.

Finally, using the short-channel subthreshold current model for subthreshold current and velocity saturation model for ON-current, the all-region short-channel I-V model is obtained by splicing them together at the threshold voltage.

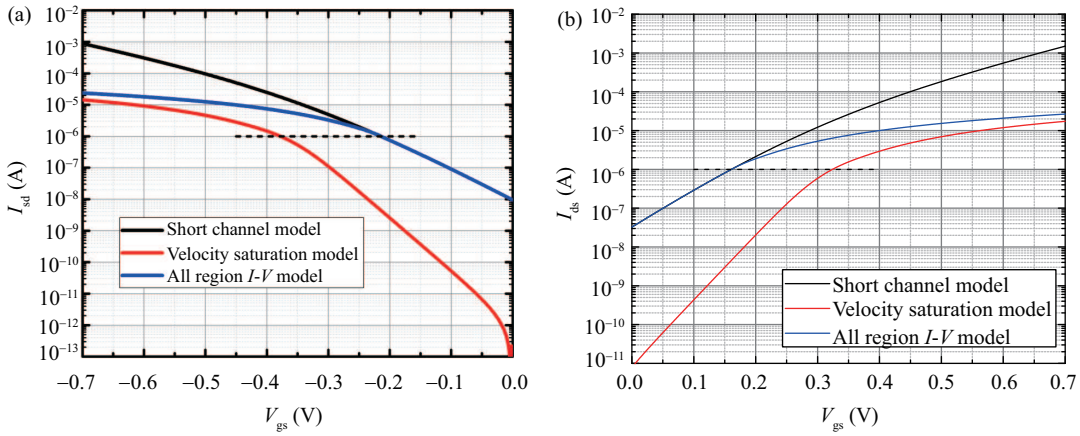

Figure 2 (Color online) (a) The I_{sd}-V_{gs} characteristic for P-type 2D DG MOSFETs (L_g = 5 nm, W = 5 nm, V_{sd} = 0.7 V); (b) the I_{ds}-V_{gs} characteristic for N-type 2D DG MOSFETs (L_g = 5 nm, W = 5 nm, V_{ds} =0.7 V).

Combined with N-type all-region short-channel I-V model for 2D DG MOSFET [10], an analytical all-region I-V model for short-channel complementary 2D MOSFETs can be obtained. By introducing a symbolic function

$$n=\begin{cases}1, & \text{N-type},\\ -1, & \text{P-type}.\end{cases} \tag{11}$$

Eqs. (2), (6), (8), (10) are rewritten using n to obtain a complementary model for both N-type and P-type 2D MOSFETs.

The inversion charge density is rewritten as

$$Q_i(x)=\frac{2\pi g_v g_s q m^* kT}{h^2}\ln\left[1+\mathrm{e}^{nq[\psi(x)-V(x)]/kT}\right]. \tag{12}$$

The current expression for short channel is

$$I_{ds}=\mu W\frac{2\pi g_v g_s m^*(kT)^2}{h^2}\frac{n[1-\mathrm{e}^{-nqV_{ds}/kT}]}{\int_0^L \mathrm{e}^{-nq\psi(x)/kT}\mathrm{d}x}. \tag{13}$$

The $V\sim\psi$ relationship in velocity saturation model can be expressed as follows:

$$V=\psi-n\frac{kT}{q}\ln\left\{n\exp\left[\frac{h^2C_{OX}}{g_v g_s\pi q m^* kT}(V_{gs}-\Delta\phi-\psi)\right]-1\right\}. \tag{14}$$

Further the velocity saturation current is

$$I_{ds}=\frac{\mu_0 W}{L+n(\mu_0/v_{sat})(\psi_d-\psi_s)}\int_{\psi_s}^{\psi_d}Q_i\frac{\mathrm{d}V}{\mathrm{d}\psi}\mathrm{d}\psi. \tag{15}$$

Figure 2 shows the transfer characteristic curves for P-type and N-type 2D DG MOSFETs calculated using the complementary I-V model. The dash lines show the position where to splice the short-channel model and velocity saturation model. The all-region model is obtained by shifting the velocity saturation model to the short-channel model and splicing them together. In detail, the points on the two models where I_{ds} and $\mathrm{d}I_{ds}/\mathrm{d}V_{gs}$ are equal, and each point corresponds to a V_{gs} value in the two drain current curves. Then, the I-V curve of velocity saturation model is shifted by the V_{gs} difference between the two models where I_{ds} and $\mathrm{d}I_{ds}/\mathrm{d}V_{gs}$ are equal, and the continuous all-region model is obtained. In this way, both I_{ds} and $\mathrm{d}I_{ds}/\mathrm{d}V_{gs}$ of all-region model are continuous. The splicing point is around the threshold voltage determined by the short-channel model and the current is about 10^{-6}A for W/L=1.

The effect of channel length on the I_{ds}-V_{gs} characteristic of N-type 2D DG MOSFET is shown in Figure 3(a). In the subthreshold region, L_g = 10 nm curve shows the effect of short-channel effect, and

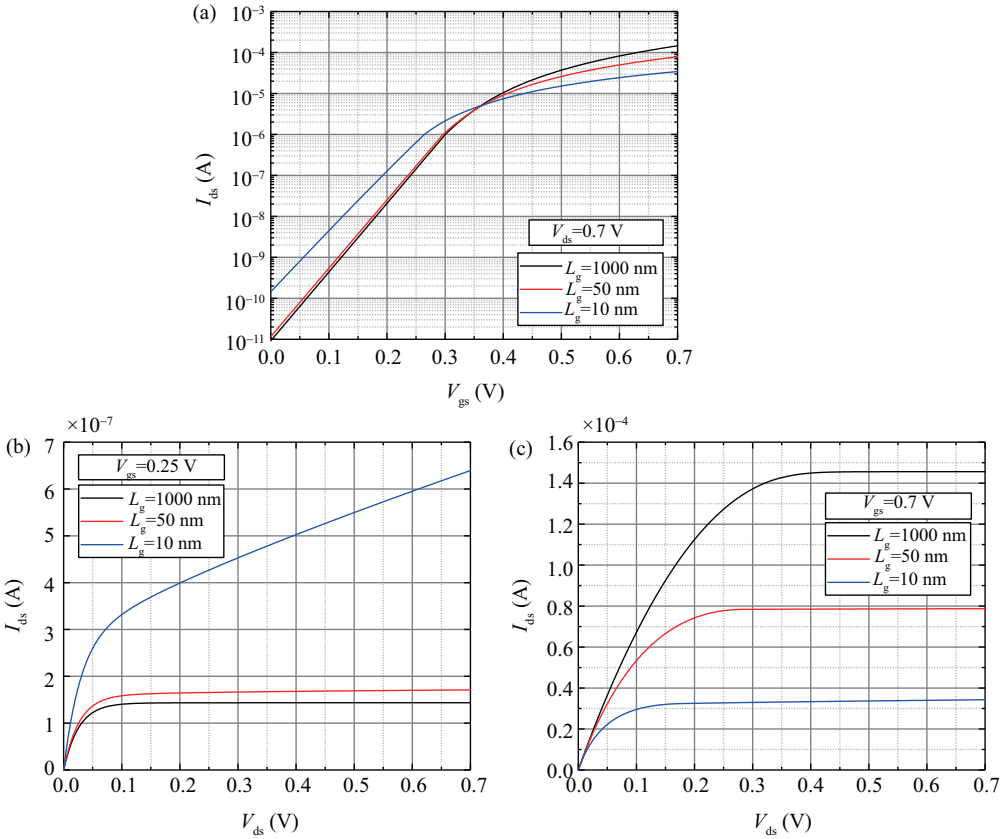

Figure 3 (Color online) (a) I_{ds}-V_{gs} characteristic of N-type 2D DG MOSFET with different channel lengths; (b) I_{ds}-V_{ds} characteristic with different channel lengths at V_{gs} = 0.25 V; (c) I_{ds}-V_{ds} characteristic with different channel lengths at V_{gs} = 0.7 V. The widths of all devices in the figure are equal to their channel length to normalize the current.

SCE makes the current higher than other curves. At the turn-on region, the velocity saturation lowers the mobility; therefore the current decreases with the decrease in channel length. Figure 3(b) and (c) exhibits the I_{ds}-V_{gs} characteristic of N-type 2D DG MOSFETs with different channel lengths. The curves at subthreshold (V_{gs} = 0.25 V) and turn-on region (V_{gs} = 0.7 V) also reflect the effect of short-channel effect and velocity saturation.

3 The short channel effects on the SNM

The basic circuit structure of a 6T SRAM is shown in Figure 4. SNM is defined as the maximum noise voltage that can be tolerated to V_1 and V_2 before the state change [15]. For the inverter composed of three transistors on each side, the butterfly curve can be calculated by applying the all-region model. Once the butterfly curves are obtained, the SNM can be received by shifting one curve left and another curve up at the same step until two curves are tangent as shown in Figure 5. The arrows point to the direction where the curves move, and the dashed line is the result of shifting. The side length of square in Figure 5 means the value of SNM.

With the scaling down of devices, the channel length of devices decreases. As the described in the previous section, the decrease in channel length decreases the current due to the effect of velocity saturation in the turn-on region, and the current increases owing to the short-channel effect at the subthreshold region. This results in the variation of threshold voltage of transistors and changes the SNM.

Figure 6(a) shows the trend of SNM with channel length. There is an optimal value of channel length L_{opt}. When the channel length is larger than L_{opt}, the SNM slightly increases with the decrease in channel length due to the effect of velocity saturation. When the channel length is smaller than L_{opt},

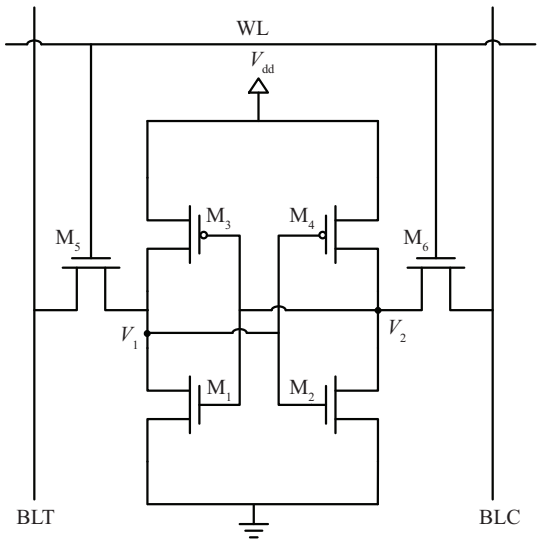

Figure 4 Circuit structure of 6T SRAM.

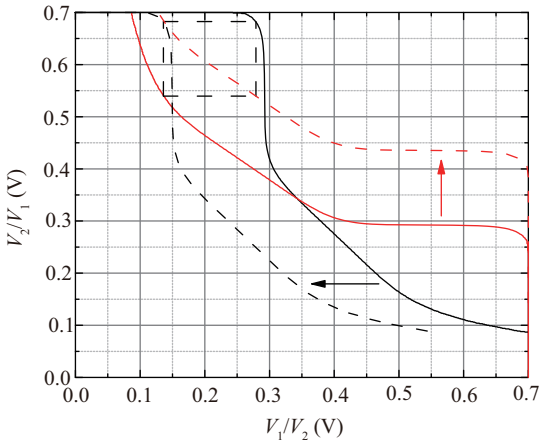

Figure 5 (Color online) Curves of SNM and the way to obtain SNM value. The W/L ratios of transistors are set as $W_1/L_1 = 4.5$, $W_3/L_3 = 1$, $W_5/L_5 = 3$ to make the curves symmetrical. The insulators of transistors are 2.5 nm thickness HfO_2.

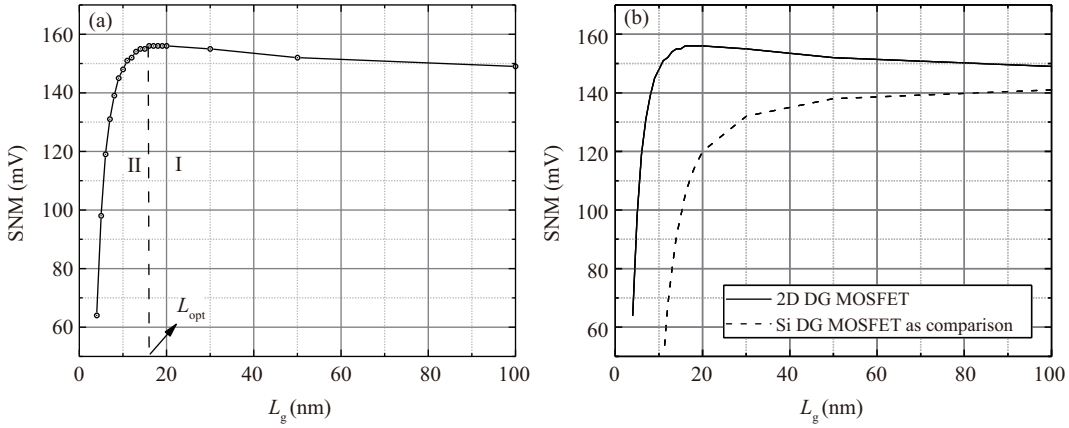

Figure 6 (a) SNM with various channel lengths; (b) comparison of SNM between SRAM cell composed of 2D DG MOSFETS and Si DG MOSFET.

obviously the SNM decreases with the decrease in channel length because the SCEs become significant. $L_{\rm opt}$ is approximately three times the scale length and divides Figure 6(a) into two regions. Region I is the region on the right of $L_{\rm opt}$, where the dominant effect is velocity saturation. Region II is the region on the left of $L_{\rm opt}$, where SCE is dominant. The difference of butterfly curves caused by channel length shrinking can be observed in Figure 7.

Figure 6(b) shows a comparison between the SNM of SRAM cell composed of 2D DG MOSFETs and Si DG MOSFETs. The SNM of Si DG MOSFETs SRAM is obtained by applying the all-region model composed of an SCE model [16] and a long-channel model [17] for Si DG MOSFETs. The channel thickness of Si DG MOSFET is 5 nm, and the thickness of HfO_2 gate insulators is 2.5 nm. The threshold voltages of transistors are adjusted to 0.3 V; they are same as 2D MOSFETs. As shown in Figure 6(b), the SNM of Si DG MOSFETs SRAM decreases more rapidly when the channel length decreases. This is because the 2D DG MOSFETs have a better control of channel when the channel length is reduced and suffer less SCEs.

In Figure 7(a), the butterfly curves in region I are shown. In this region, the decrease in channel length

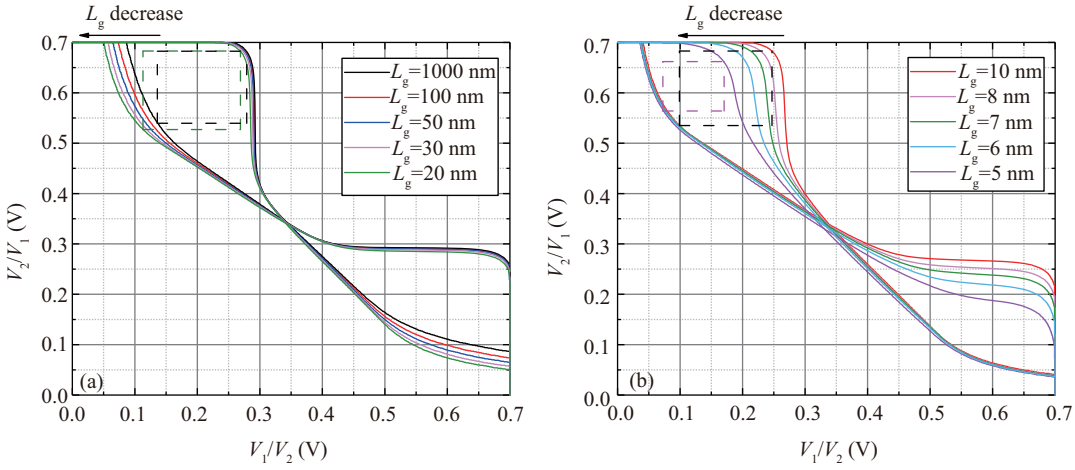

Figure 7 (Color online) (a) SNM curves with the decrease in channel length (velocity saturation is dominant); (b) SNM curves with the decrease in channel length (short-channel effect is dominant).

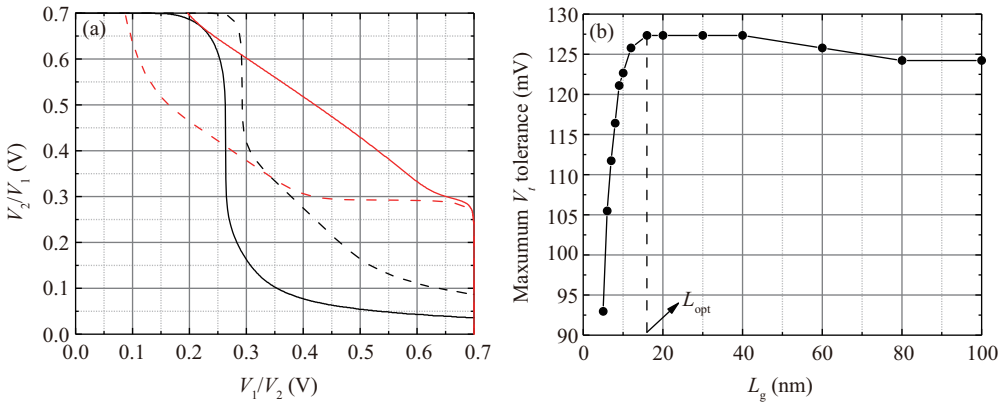

Figure 8 (Color online) (a) SNM vanishes due to technology fluctuation; (b) maximum threshold voltage tolerance with the change in channel length. The dash lines show the butterfly curves when all the transistors have the same threshold voltage. The solid lines show the occurrence of SNM vanishing.

increases the electric field, resulting in the decrease of mobility. The decrease in mobility decreases the current and leads to an increase in threshold voltage. In the area where curves obviously change, the voltage drop on access transistor is larger than that drop on pull-down transistor. Therefore, with the decrease in channel length, the access transistor will suffer more velocity saturation than the pull-down transistor, and the current decrease ratio of access transistor is larger. This affects the voltage division between these two transistors and increases the voltage drop on access transistor. As a result, the SNM slightly increases with the decrease in channel length.

Figure 7(b) shows the butterfly curves in region II. In this region, with the contribution of short-channel effects, the current increases with the decrease in channel length, and the threshold voltage decreases with the decrease in channel length. As shown in Figure 7(b), the decrease in threshold voltage makes the maximum square in butterfly curves getting smaller and results in the decrease of SNM.

In semiconductor manufacturing, the technology fluctuation may make the threshold voltage of transistors deviate from the designed value [18]. The value of SNM becomes the worst when the threshold voltage fluctuations of transistors in two inverters in 6T SRAM are exactly mismatched [19]. In this case, the fluctuation value that makes SNM vanish is the maximum threshold voltage tolerance of 6T SRAM, as shown in Figure 8(a).

As the scaling down of devices, the maximum threshold voltage tolerance is also affected by velocity saturation and short-channel effects. Figure 8(b) indicates the maximum threshold voltage tolerance with the change in channel length. Similar to the previous discussion, the maximum threshold voltage

tolerance first becomes slightly larger with the decrease in channel length, because the velocity saturation makes the current of transistor smaller and increases the threshold voltage. When the short-channel effect is dominant, the maximum threshold voltage tolerance decreases with the decrease in channel length, as the short-channel effect makes the threshold voltage smaller. There is still an optimal value of channel length about three times the scale length, making maximum threshold voltage tolerance maximum.

4 Conclusion

This work studies the influence of SCEs on the SNM of 6T SRAM composed of 2D MOSFETs. An analytical all-region I-V model for short-channel complementary 2D MOSFETs has been developed. A method to simulate the SNM of 6T SRAM through this all-region model has been built. With the consideration of SCEs and velocity saturation, an optimal value of channel length $L_{\rm opt}$ that makes the SNM of 6T SRAM achieve the maximum value is found at about three times the scale length. When the channel length is larger than $L_{\rm opt}$, SNM slightly increases as L decreases because of velocity saturation. When channel length is smaller than $L_{\rm opt}$, SNM rapidly decreases as L decreases as SCEs are dominant. The worst case of SNM reduction due to V_T fluctuation is investigated. In an SRAM with a scale length of 5 nm, the maximum V_T tolerance decreases from 126 to 105 mV when L decreases from 15 to 5 nm.

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