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Modeling of program Vth distribution for 3-D TLC NAND flash memory

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Abstract This paper proposes a simulation method to model the program Vth distribution of 3-D vertical channel TLC/QLC charge-trapping NAND flash memory. The program Vth distribution can be calculated by considering ISPP noise, WL-WL interference, and the RTN effect of tunneling oxide and poly Si, which are the major physical factors affecting the width of program Vth distribution. Then, the program Vth distribution shapes with different ISPP incremental voltage steps are compared, and the results are found to be consistent with the experimental results. Code and layer-dependent coupling coefficients of WL-WL interference in 3-D vertical channel NAND flash memory are considered. The effect of RTN on the program Vth distribution is comprehensively studied. The program Vth distribution of a WL is calibrated with the measurement, and a good agreement is obtained, validating the array program Vth distribution simulation method. The simulation method can help in improving the reliability of 3-D TLC NAND flash memory and provides guidance for the design and optimization of 3-D QLC NAND flash memory technology.

Keywords modeling and simulation, measurement, reliability, program Vth distribution, charge-trapping memory, 3-D vertical channel TLC/QLC NAND flash memory

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1 Introduction

With the intensive application of data storage in emerging technologies, 3-D NAND flash memory technology has been considered as a promising candidate for future memory solutions [1–5]. This is because it overcomes many challenges faced by conventional planar (2-D) NAND flash memory [6, 7] and meets the requirements for mass storage devices [8]. At present, 48, 64, and even 96-stacked layer 3-D TLC NAND flash memories are produced [8–12].

Despite the several advantages of 3-D NAND flash memory, its reliability degrades with the continued scaling down and introduction of multi-level cell (MLC) and triple-level cell (TLC) NAND flash memory technologies [13, 14]. In particular, the transition from 2-D NAND flash memory to 3-D NAND flash memory has been raising many new challenges [15]. 3-D quad-level cell (QLC) NAND flash memory technology is a promising candidate for lower cost per bit and higher-density nonvolatile memory [16,17]. However, for 3-D TLC and QLC NAND flash memories, a narrow program Vth distribution interval is very important. Therefore, minimizing the width of the program Vth distribution is a central challenge for multi-bit storage technology. In order for minimization to occur, it is necessary to identify and understand the effect of different physical factors on the program Vth distribution width [18]. After this,

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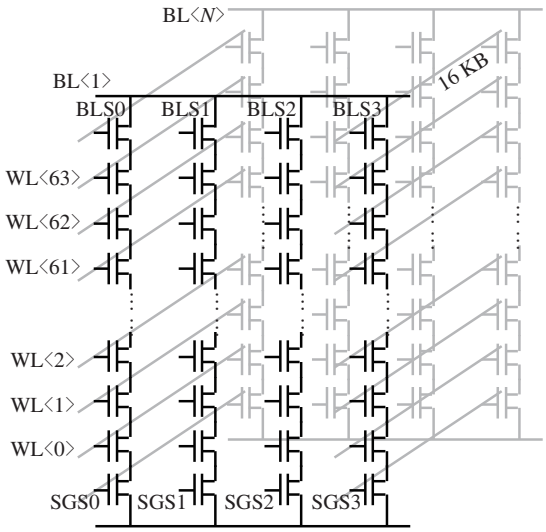

Figure 1 Schematic structure of 64-stacked layer 3-D vertical channel TLC charge trapping NAND flash memory array in a block.

modeling the accuracy of the Vth distribution of 3-D TLC NAND flash memory can make the design of error correction codes (ECCs) more accurate and efficient. However, it takes considerable time to obtain the program Vth distribution based on large-scale measurements. Therefore, modeling the program Vth distribution can make the process more effective and efficient [19].

In this paper, a simulation method is proposed to model the program Vth distribution of 3-D vertical channel (VC) TLC/QLC charge-trapping (CT) NAND flash memory, considering ISPP (incremental step pulse programming) noise, WL-WL (word-line) interference, and the RTN (random telegraph noise) effect of tunneling oxide and poly Si, which are the major physical factors that affect the width of the program Vth distribution. After the model is created, the program Vth distribution shapes with different ISPP incremental voltage steps (Vsteps) are compared, and different Vth distribution shapes (rectangle and triangle) are observed, which is consistent with the experimental results. Code and layer-dependent coupling coefficients of WL-WL interference in 3-D VC NAND flash memory are considered. Finally, the effect of RTN on the program Vth distribution is comprehensively studied, and different program/erase (P/E) cycling times and ambient temperatures can be considered. The program Vth distribution of a WL is calibrated with the measurement, and a good agreement is obtained, which validates the array program Vth distribution simulation method. The simulation method can help in improving the reliability of 3-D TLC NAND flash memory and provides guidance for the design and optimization of 3-D QLC NAND flash memory technology.

The rest of this paper is organized as follows. In Section 2, we describe the 64-stacked layer 3-D VC TLC CT NAND flash memory array structure and program Vth distribution simulation method; in Section 3, we present the simulated and experimental results and discussion; finally, the conclusion is drawn in Section 4.

2 Array structure and simulation method

The proposed simulation method is universal for different 3-D NAND flash architectures. Thus, we can use the mainstream 3-D TLC NAND flash memory architecture [10, 11] as an example to explain the simulation method in this study. Figure 1 shows a typical schematic structure of a 64-stacked layer 3-D VC TLC CT NAND flash memory array in a block. Figure 2 shows the Vth distribution, read voltage window, and page configuration of the 3-D TLC NAND flash memory. 3-D TLC and QLC NAND flash memories require extremely narrow program Vth distribution compared to the single-level cell (SLC) and MLC NAND flash memory. Three major obstacles against enabling narrow program Vth distribution,

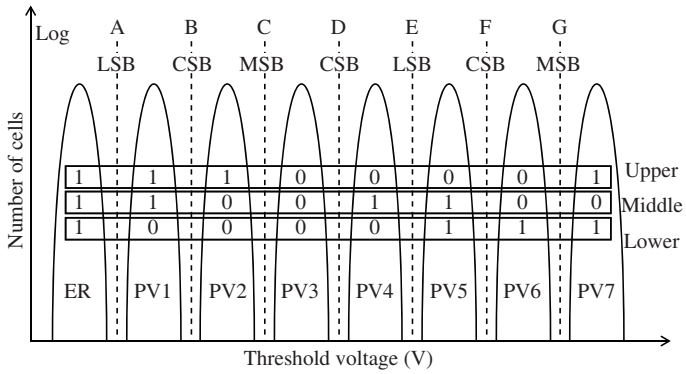

Figure 2 Vth distribution, read voltage window, and page configuration of the 3-D TLC NAND flash memory.

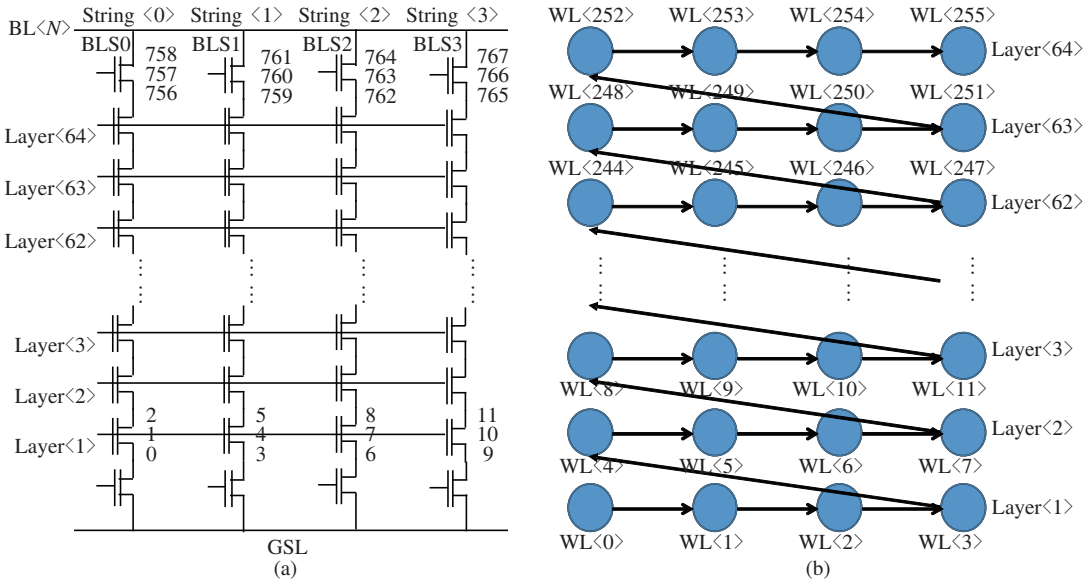

Figure 3 (Color online) Block page order (a) and the program sequence (b) of the 3-D VC TLC NAND flash memory.

consisting of ISPP noise, WL-WL interference, and the RTN effect of tunneling oxide and poly Si, are comprehensively studied.

The block page order and the program sequence of the 3-D VC TLC NAND flash memory array are shown in Figure 3(a) and (b). Here, a block is defined as 255 WL (4 strings and 64 layers), where one WL's (three pages) length is 16 KB [10, 11]. A block is the smallest unit for erase operation before the ISPP program, and the Vth distribution of the erased memory cells tend to have a wide-Gaussian distribution [20, 21]. Thus, we first initialize the Vth of every cell in a block to be in the erase state, whose Vth distribution follows a normal distribution ($\mu = -3$ [19], $\sigma = 0.21$ [22]). Contrary to the ISPP program sequence of the actual array program operation, we program a block from WL$\langle 255\rangle$ to WL$\langle 0\rangle$ due to the directionality of WL-WL interference, namely, the former programmed cell's Vth can be affected by the latter programmed cell's Vth, and it can also be related with the Vth shift of the latter programmed cell. The flowchart of the array program Vth distribution simulation method of 3-D TLC NAND flash memory is shown in Figure 4.

2.1 ISPP noise

ISPP noise originates from the variation of the number of electrons in the nitride layer [23], which has an essential effect on the program Vth distribution. Figure 5 plots the ISPP program result of the single memory cell, where a self-consistent simulator is used to simulate the program, erase, retention, and read operations, as verified and calibrated in our previous studies [24–27]. The figure indicates that the ISPP

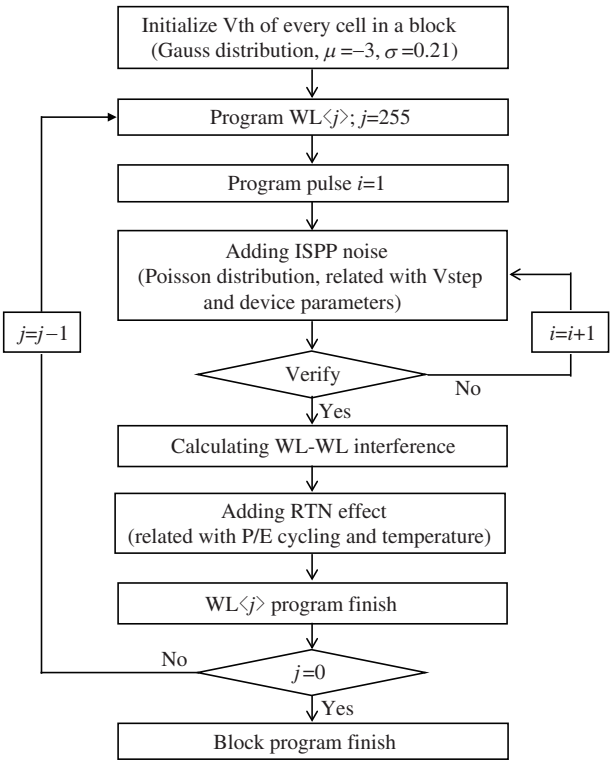

Figure 4 Flowchart of the array program Vth distribution simulation method of 3-D TLC NAND flash memory.

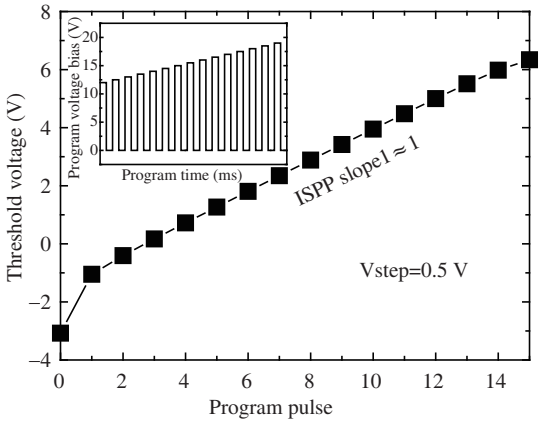

Figure 5 Single memory cell programming characteristic by ISPP. The program voltage is 8–18 V, and the adopted program pulse is shown in the insert.

slope is around 1 due to the limitation of the tunneling current [28]. Thus, ideally, the program voltage distribution is a uniform distribution between Vpv and Vpv+Vstep. However, in reality, a positive tail above Vpv+Vstep is introduced by ISPP noise. Figure 6(a) shows the typical Vth distribution shift of the 3-D NAND flash memory array during dumb ISPP program (without a verify operation) [19], and the distribution is moved to the right and broadened pulse-by-pulse. For each ISPP program step, the Monte Carlo method [29] is used to generate a Vth shift randomly for each cell in the block whose probability distribution follows Poisson statistics [23,30,31]. Figure 6(b) shows the ISPP noise with different Vsteps, and it is found that a larger Vstep has larger ISPP noise. The ISPP noise originates from the variation of the number of electrons in the nitride layer, and the electron injection statistics show Poisson behavior. The variance and average value of electron injection statistics are related to the Vstep and the device

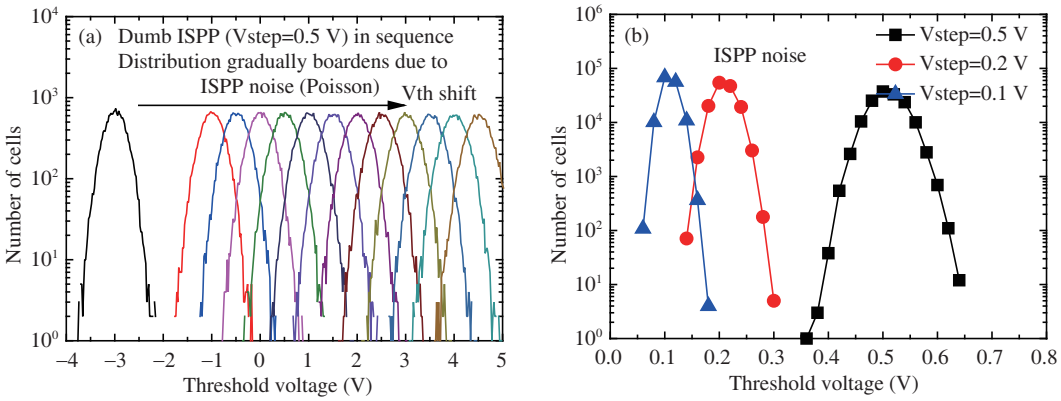

Figure 6 (Color online) (a) Typical Vth distribution shift of a 3-D NAND flash memory array during dumb ISPP program; (b) ISPP noise with different Vsteps.

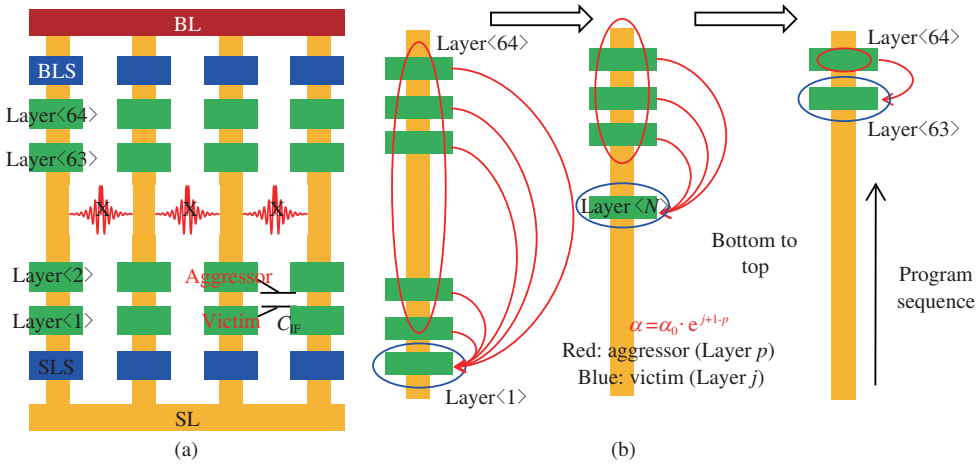

Figure 7 (Color online) (a) WL-WL interference of 3-D VC NAND flash memory because of coupling capacitance; (b) all possible cases of WL-WL interference at a single memory string in a 3-D VC NAND flash memory.

structure parameters, as follows [23]:

$$\bar{n} = V_{\text{step}}/C_{\text{PP}}, \tag{1}$$

$$\Delta V_{\text{th}} = q \cdot n/C_{\text{PP}}. \tag{2}$$

Here, q is the electronic charge, and C_{PP} is the control-gate to nitride layer coupling capacitance, which can be calibrated in combination with the measurement. In this simulation, we assume a sheet charge centroid inside the nitride layer. Then, $\bar{n}$ is the average value of the injected electrons, and n is the number of injected electrons. Because of the electron injection statistics according to Poisson behavior, its variance σ_n^2 is equal to the average value $\bar{n}$.

2.2 WL-WL interference

WL-WL interference is also an important factor that affects the array program Vth distribution. Figure 7(a) shows the WL-WL interference of 3-D VC NAND flash memory caused by the coupling capacitance (C_{IF}), which is immune to the WL-WL interference between the string and the string due to the source line slits inside the array [8]. Then, we can find that the memory cell located in layer 1 suffers from as much as 63 times WL-WL interference, while that located in layer 64 is immune to WL-WL interference due to the directionality of the program sequence, as shown in Figure 7(b). In addition, the Vth shift of the victim cell is related to the PV level of the victim cell and the target Vth its neighboring cell programmed to [32, 33]. Finally, we can find that WL-WL interference causes Vth shift of a single

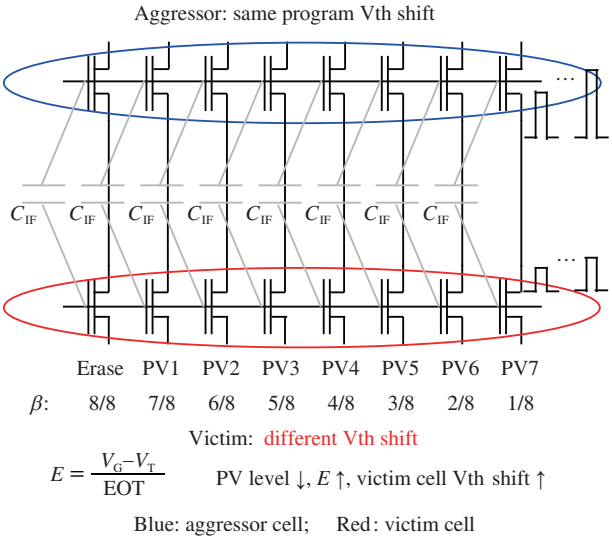

Figure 8 (Color online) Vth shift of victim cell due to WL-WL interference in correlation with the PV level of the victim cell.

cell (victim cell) proportional to the Vth change of the adjacent cell (aggressor cell), and is related to the PV level of the victim cell and the distance between the victim cell and aggressor cell. Here, we define the coupling degree related to the distance as α (layer-dependent coefficient), which is assumed to decay exponentially, as shown in Figure 7(b). The coupling degree related to the PV level of the victim cell is defined as β (code-dependent coefficient), which is assumed to be linearly dependent on the PV level, as shown in Figure 8. The coupling degree related to Vth change of the aggressor cell is defined as $\Delta V_{\text{aggressor}}$. Namely, the Vth shift of the victim cell is directly correlated with the number of ISPP programming step pulses applied to the adjacent cell [32,33]. Thus, the Vth shift of a victim cell due to interference is as follows:

$$\Delta V_{\text{victim}}(j) = \sum_{p=j+1}^{64} \alpha(p-j) \cdot \beta(j) \cdot \Delta V_{\text{aggressor}}(p). \tag{3}$$

Here, j is the victim cell layer, and p is the aggressor cell layer. Then, $\alpha = \alpha_0 \cdot \mathrm{e}^{j+1-p}$ as shown in Figure 7, where α_0 is used as 0.02 in this work, and β is 8/8, 7/8, 6/8, 5/8, 4/8, 3/8, 2/8, and 1/8 when the PV level of the victim cell in the erase state, PV1, PV2, PV3, PV4, PV5, PV6, and PV7 respectively as shown in Figure 8.

2.3 RTN effect

RTN is one of the main reliability constraints for the 2-D and 3-D NAND flash memories. RTN causes Vth instability of 3-D NAND flash memory during two consecutive read operations [34], which originates from the electron capture/release phenomena in memory cell defects of tunneling oxide and poly Si. Figure 9 shows the measured RTN statistics probability density distribution of the 3-D NAND flash memory for different ambient temperatures [15]. RTN not only widens the positive tail above the PV level, but also introduces a negative tail below the PV level [34], which significantly distorts the program Vth distribution. The probability density of RTN distribution is as follows [34]:

$$P\left[\Delta V_{\text{th}}\right] = \eta \mathrm{e}^{\pm\lambda\Delta V_{\text{th}}}. \tag{4}$$

Here, λ is the slope of the exponential tails of the RTN distribution, and η is a variable coefficient that can be calibrated with different manufacturing processes, different experimental temperatures, and P/E cycling times. Similar to ISPP noise, a Monte Carlo method is used to randomly generate a Vth shift for each cell in a block in the form of probability. The simulated Vth distribution broadening for a PV level of 2.5 V is shown in Figure 10.

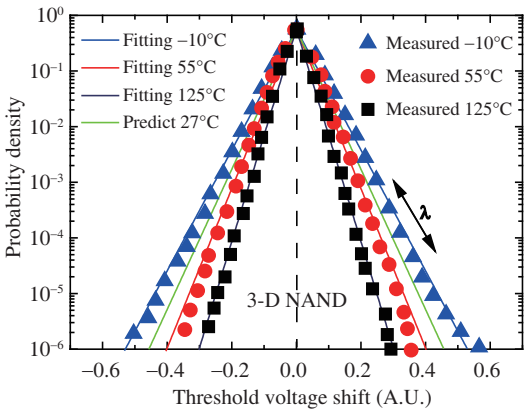

Figure 9 (Color online) RTN probability density distribution of the 3-D NAND flash memory at different ambient temperatures.

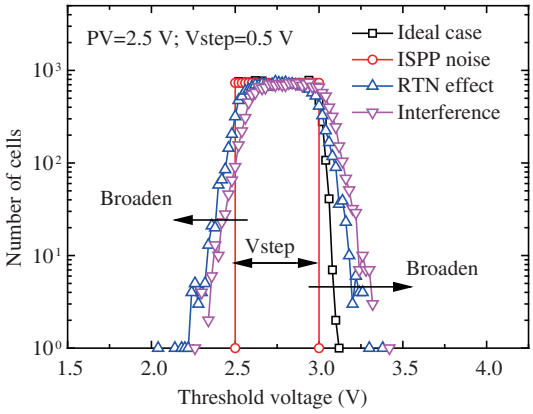

Figure 10 (Color online) Simulated Vth distribution broadening at a PV level of 2.5 V.

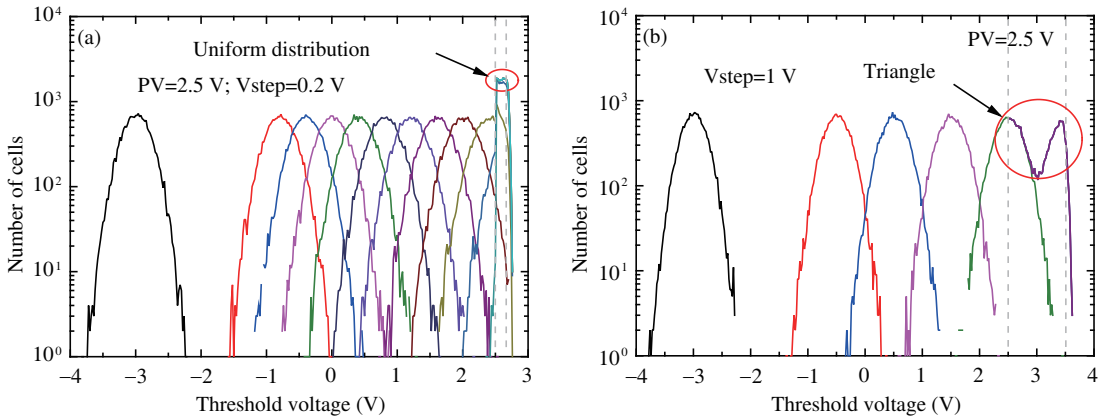

Figure 11 (Color online) Vth distribution evolutions during ISPP PV function at Vsteps of (a) 0.2 V and (b) 1 V.

3 Results and discussion

Theoretically, the Vth distribution resulting from the ISPP PV function is a uniform distribution between Vpv and Vpv+Vstep. In reality, the Vth distribution is broadened due to ISPP noise, which is the ultimate accuracy of the ISPP algorithm [23]. Figure 11(a) shows the Vth distribution evolution (sweep every two loops, without considering RTN effect) during the ISPP PV function. The PV level is 2.5 V, and Vstep is 0.2 V. The figure indicates that the uniform distribution between Vpv and Vpv+Vstep is almost maintained. However, the positive tail above Vpv+Vstep is shown due to ISPP noise. This is because a memory cell with a Vth slightly lower than Vpv requires an additional ISPP program pulse to overcome the PV level [29]. Figure 11(b) shows the influence of Vstep on the program Vth distribution, as well as how a triangle distribution is obtained [35]. It can be seen that different Vsteps can lead to different Vth distribution shapes, which is consistent with the experimental results [35].

Figure 12(a) shows the effect of RTN on the program Vth distribution, as well as the further distortion of the uniform distribution. Figure 12(b) shows the ISPP program Vth distribution shift of PV5 for both simulation and measurement, and a good agreement is obtained between the two results. Note that the experimental results of the program Vth distribution below 0 V cannot be obtained. Figure 13 shows the Vth distribution of WL$\langle 252\rangle$ on layer 64 and that of WL$\langle 0\rangle$ on layer 1 at the memory string $\langle 0\rangle$ of the 3-D VC TLC NAND flash memory, (a) considering and (b) without considering the code-dependent coefficient. The figure shows that (1) the Vth distribution of WL$\langle 252\rangle$ on layer 64 represents the relative small Vth shift compared to the Vth distribution of WL$\langle 0\rangle$ on layer 1 at the memory string$\langle 0\rangle$, due to

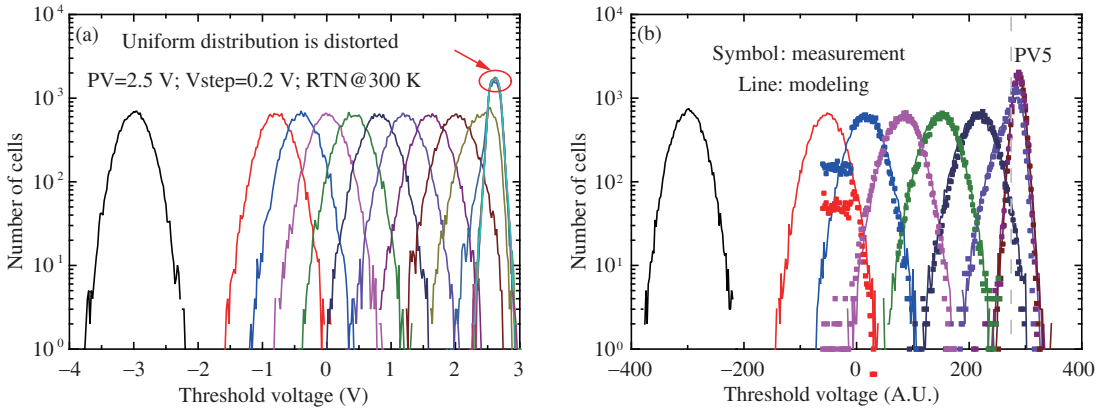

Figure 12 (Color online) (a) Effect of RTN on the program Vth distribution; (b) ISPP program Vth distribution of PV5 for both simulation and measurement, and a good agreement is obtained between the two results.

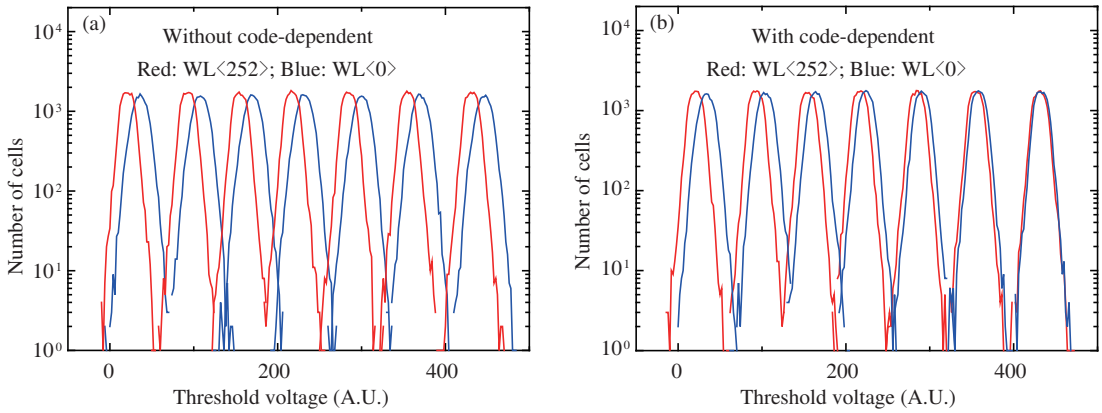

Figure 13 (Color online) Simulated Vth distributions of WL⟨0⟩ and WL⟨252⟩ at the memory string ⟨0⟩ of the 3-D VC TLC NAND flash memory (a) considering and (b) without considering the code-dependent coefficient.

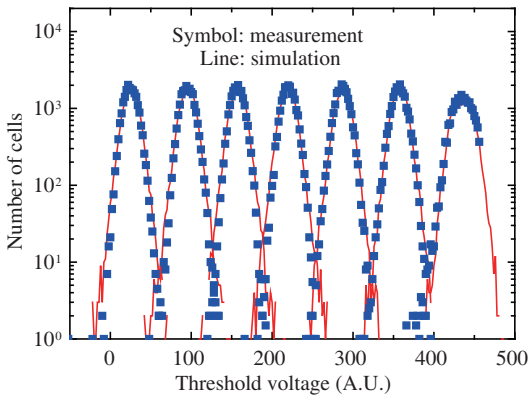

Figure 14 (Color online) Simulated Vth distribution of one page versus measured one, and a good agreement is obtained between the two results.

the directionality of WL-WL interference; (2) WL-WL interference of the erase state cell is larger than that of the program state cell. The simulated Vth distribution of one page versus the measured one is calibrated with the experimental measurements combined with the double-verify algorithm [36], as shown in Figure 14, and a good agreement is obtained between the two. This validates the array program Vth distribution simulation method.

4 Conclusion

This paper proposes a simulation method to model the program Vth distribution of the 3-D vertical channel TLC/QLC charge-trapping NAND flash memory. The program Vth distribution can be calculated by considering ISPP noise, WL-WL interference, and the RTN effect of tunneling oxide and poly Si, which are the major physical factors that affect the width of the program Vth distribution. The ISPP program results obtained with different Vsteps are compared, and different Vth distribution shapes are observed, which is consistent with the experimental results. Code and layer-dependent coupling coefficients of WL-WL interference in the 3-D VC NAND flash memory are considered. The effect of RTN on the program Vth distribution is comprehensively studied. The program Vth distribution of a WL is calibrated with the measurement, and a good agreement is obtained, which validates the array program Vth distribution simulation method. This simulation method can help in improving the reliability of 3-D TLC NAND flash memory and provides guidance for the design and optimization of 3-D QLC NAND flash memory technology.

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