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A Qi compatible wireless power receiver with integrated full-wave synchronous rectifier

Chubin WU, Zhang ZHANG*, Jianmin ZENG, Xin CHENG & Guangjun XIE

School of Electronics Science and Applied Physics, Hefei University of Technology, Hefei 230009, *China*

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Dear editor,
Wireless power transfer (WPT) is widely used in recent years [1]. Many applications, such as biomedical implants, battery chargers of portable electronic devices and electric vehicles already adopt [2–4] or will adopt [5] this approach. Industry consortia, such as the wireless power consortium (WPC), have been established to regulate inductively coupled power transfer applications. The specification issued by the WPC is the Qi standard. All the applications, whether they are transmitters or receivers, following the Qi standard can work compatibly.

In this study, a Qi compatible wireless power receiver is proposed. The receiver adopts four high-voltage N-channel MOSFETs to rectify the AC power from the coil that can improve the power conversion efficiency (PCE) and minimize the chip area compared to P-channel MOSFETs or passive diodes [6]. The four MOSFETs are controlled by a synchronous controller, which is proposed to turn on and off each MOSFET synchronously to the polarity of the received AC signal. The proposed synchronous controller includes a digital pulse width controller, and it is used to compensate the turn-off delay of the MOSFET, which can effectively prevent the reverse leakage current and improve the receiver efficiency.

The grey part of Figure 1 illustrates the block diagram of the proposed synchronous rectifier. The rectifier is composed of four high-voltage MOSFETs (MOS1, MOS2, MOS3 and MOS4), a system power generator, two high-side MOS drivers (DRV1 and DRV2), two low-side MOS drivers (DRV3 and DRV4), two Schottky diodes (D1 and D2), two resistors (R1 and R2), and a synchronous controller. Each of the MOSFETs is driven by a MOS driver, and all of the MOS drivers are controlled by a synchronous controller.

The main working process of the synchronous rectifier is as follows. At the start up, the receiver is at the zero-power state. When the receiver is placed on a transmitter and the transmitter is powered up, the coil in the secondary part induces AC power. The four MOSFETs in the receiver work as passive diodes and rectify AC power to DC power. When the system power generator is powered up, it generates the system power VCC_SYS. Then the rest parts of the receiver system start working.

Because the four MOSFETs are all N-channel, to open the two high-side MOSFETs, their gate drive voltage must be high enough. Here, we use two off-chip bootstrap capacitors C1 and C2 to boost up the voltage of BOOT1 and BOOT2, respectively, which are the input power of the two high-side MOS drivers. The working principle of the two bootstrap capacitors C1 and C2 is as follows: the Schottky diode D1 between VCC_SYS and BOOT1 and the Schottky diode D2 between VCC_SYS and BOOT2 give the initial voltage VBOOT_Initial to BOOT1 and BOOT2,

* Corresponding author (email: zhangzhang@hfut.edu.cn)

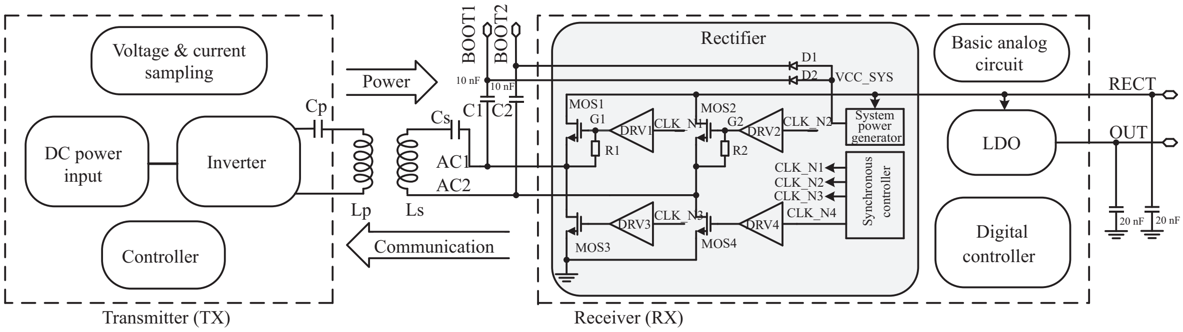

Figure 1 The system architecture of the proposed wireless power receiver.

respectively, so that the VBOOT_Initial is close to VCC_SYS. When the AC (AC1 or AC2) input is low, the BOOT (BOOT1 and BOOT2) voltage is equal to VBOOT_Initial. When the AC is high, the BOOT voltage is bootstrapped to AC+ VBOOT_Initial through the bootstrap capacitors; therefore, the voltage of BOOT can ensure that the gate-voltage to drive the high-side MOSFETs open. After the receiver system is powered up, the synchronous controller starts working. The function of the synchronous controller is to control each of the MOSFETs synchronously turn-on and turn-off according to the polarity of the received AC signal.

The synchronous controller is composed of several parts, including two low-side voltage comparators, two high-side voltage comparators, two digital pulse width controllers, and a non-overlapping clocks generator. The high-side comparators are used to compare the input AC signal with the rectified voltage RECT, while the low-side comparators are used to compare the input AC signal with the ground voltage. The outputs of these voltage comparators are the main input signals of the non-overlapping clocks generator. The relationship of all these modules can be found in supporting information.

The proposed digital pulse width controller is used to control the maximum effective pulse width of the synchronous rectifier. Unlike the passive diodes, the current flow of the MOSFETs is bidirectional. If the timing of the MOSFETs turn-on and turn-off is not controlled correctly, the turn-off delay may be introduced by the comparators, the logical circuit, and the MOS drivers, and the current may flow from the DC output to the AC input. This reverse leakage current severely degrades the power conversion efficiency [7, 8]. Since the turn-on delay will not cause any reverse leakage current, we do not need to consider this problem.

The digital pulse width controller uses the previous AC signal high-level width to generate a high pulse in the current AC cycle, and the high pulse output is shorter than the previous AC signal high-level width. Before the AC signal changes from a high level to a low level, the high-pulse signals control the relevant high-side power MOSFETs through the non-overlapping clocks generator to shut off. This can effectively eliminate the turn-off delay of the MOSFETs, prevent the reverse leakage current, and improve the system efficiency.

The chip is fabricated with the TSMC 0.18 μm 1 poly 4 metal BCD process, and the chip microphotograph occupies 9.9 mm^2. The peak power efficiency of the wireless power system is 82% at 0.9 A, 5 V output, and the efficiency is higher than 70%, when the output current is above 0.3 A.

Conclusion and future work. This study presents a wireless power receiver with an improved full-wave synchronous rectifier. In the synchronous receiver, a digital pulse width controller is described to compensate the turn-off delay introduced by the comparators, logical circuit, and drivers. In this way, the pulse width controller effectively prevents the reverse leakage current. The proposed synchronous receiver leads to the state-of-the-art performance with the receiver demonstrating about 82% efficiency from the output at 0.9 A and 5 V. The efficiency is higher than 70%, when the output current is above 0.3 A. This extends applications of the receiver in different products.

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Supporting information Appendixes A, B. The supporting information is available online at info. scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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